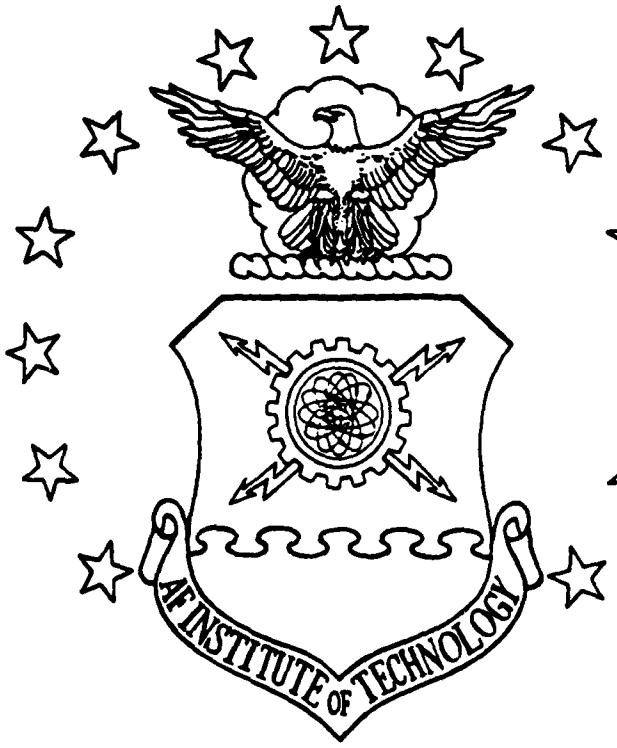
(1)



INVESTIGATION OF A SELF-ALIGNED, STRAINED-CHANNEL, n^+-InAs/$Al_{0.5}Ga_{0.5}As$/ $In_{0.15}Ga_{0.85}As$ SEMICONDUCTOR INSULATOR SEMICONDUCTOR FET (SISFET)

THESIS

David W. Rapp, B.S.E.E.
Captain, USAF

AFIT/GE/ENG/88D-40

DEPARTMENT OF THE AIR FORCE

AIR UNIVERSITY

AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

AFIT/GE/ENG/88D-40

INVESTIGATION OF A SELF-ALIGNED, STRAINED-CHANNEL, n^+-InAs/$Al_{0.5}Ga_{0.5}As$/ $In_{0.15}Ga_{0.85}As$ SEMICONDUCTOR INSULATOR SEMICONDUCTOR FET (SISFET)

THESIS

David W. Rapp, B.S.E.E.
Captain, USAF

AFIT/GE/ENG/88D-40

AFIT/GE/ENG/88D-40

INVESTIGATION OF A SELF-ALIGNED, STRAINED-CHANNEL, n^+-InAs/$Al_{0.5}Ga_{0.5}As$/$In_{0.15}Ga_{0.85}As$ SEMICONDUCTOR INSULATOR SEMICONDUCTOR FET (SISFET)

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

David W. Rapp, B.S.E.E.
Captain, USAF

November 30, 1988

Preface

An attempt was made to fabricate a self-aligned, strained-channel, SISFET from MBE grown layers of InAs, $Al_{0.5}Ga_{0.5}As$, and $In_{0.15}Ga_{0.85}As$ on GaAs. Although some devices exhibited transistor action, none carried sufficient current. Specific contact resistances of 0.65 $\Omega \cdot mm$ were achieved. A TEM analysis confirmed that one of the problems was faulty MBE growth. A classical statistics charge-control model was developed which provides the theoretical basis for the study. These derivations and calculations extend to predictions for the threshold voltage, gate leakage, and I-V characteristics for the pseudomorphic SISFET.

Providentially, I had a knowledgeable and distinguished thesis committee. My thesis advisor, Major Donald R. Kitchen, provided guidance, teaching, encouragement, and evaluation. I am especially grateful to him for this backing, which he willingly provided, even at his own time and expense. My sponsor, Dr. Cole W. Litton, from the Avionics Laboratory provided daily encouragement and coordinated the fabrication process. His operational expertise is without parallel. Major Edward S. Kolesar challenged me to learn, both in this effort and in his classroom. My sincere appreciation goes to Captain Randy J. Jost and Captain Bill R. Hodges as well as the rest of the committee for their constructively critical review of the manuscript.

I am indebted to Professor Hadis Morkoç and his students at the Coordinated Sciences Laboratory, University of Illinois at Urbana-Champaign. His originality produced many of the ideas of this effort, and he provided the use of the device fabrication facilities. My sincere thanks goes to Jim Chen for his willing assistance in the device fabrication process and to Chin-Kun Peng for useful discussions.

Thanks go to Don Smith and Bill Trop in the AFIT Microelectronics Laboratory for the SEM work. Several individuals from the Air Force Avionics Laboratory assisted me with device fabrication and characterization. Thanks go to: Mike Cheny, John Christ, Ed Davis, Jim Farmer, Edgar Martinez, Mike Paulus, Eric Taylor, and George Wilder. Several individuals from the Materials Laboratory assisted me with TEM characterization. Hearty thanks go to: Scott Apt, Cheryl Heidenreich, Alan Jackson, Pam Lloyd, and Ralph Omlor.

I wish to thank my parents for their guidance and support. Finally, simple thanks are insufficient for my wife, Kimberly, whose noble character and unwavering support bring substance to our home. This thesis is dedicated to her.

My motivation for this effort was for the greater glory of the one and only, living and true God, who exists in three persons: the Father, maker of heaven and earth; the Son, Jesus Christ, my saviour and king; and the Holy Spirit, who proceeds from the Father and the Son.

Table of Contents

List of Figures

List of Tables

List of Symbols

Symbol	Description	Unit
A	Surface area of gated region	cm^2
a_o	Equilibrium lattice constant	Å
α_n	Airy equation constant for n^{th} sub-band energy level in quantum potential well	$V \cdot m^{4/3}$
D	Electric displacement vector	$Coul/cm^2$
D	Density of states in quantum potential well	$(V \cdot m^2)^{-1}$
d	Thickness of AlGaAs barrier layer	Å
d_i	Interatomic spacing between lattice planes	Å
dl	Differential vector along path of integration	cm
ds	Differential vector normal to surface of integration	cm
E	Electric field vector	V/cm
E_c	Conduction band energy level	V
E_{fi}	Fermi energy level with respect to conduction band energy level in the channel at the heterointerface	V
E_n	Energy level of n^{th} sub-band in quantum potential well with respect to conduction band energy in the channel at the heterointerface	V
E_x	Magnitude of electric field in x direction	V/cm
E_y	Magnitude of electric field in y direction	V/cm
E_z	Magnitude of electric field in z direction	V/cm
ΔE_c	Heterojunction conduction band discontinuity	eV

ΔE_g	Heterojunction band gap energy difference	eV
ϵ	Permittivity of a material	F/cm
ϵ_{Al}	Permittivity of $Al_xGa_{1-x}As$	F/cm
ϵ_{In}	Permittivity of $In_yGa_{1-y}As$	F/cm
f_{max}	Maximum frequency of oscillation	Hz
f_t	Forward current-gain cutoff frequency	Hz
F	An applied gate field	V/m
ϕ_1	Conduction band energy discontinuity at the gate/AlGaAs heterointerface	V
ϕ_2	Conduction band energy discontinuity at the AlGaAs/channel heterointerface	V
ϕ_3	Conduction band energy discontinuity at the channel/GaAs heterointerface in a pseudomorphic structure	V
ϕ_B	Barrier to gate leakage current (perpendicular transport) in a SISFET (equals ϕ_2-E_{fi})	V
g_m	Transconductance	mS/mm
g_{mo}	Intrinsic transconductance (equals $[g_m^{-1}-R_{cs}]^{-1}$)	mS/mm
$\hbar$	Reduced Plank's constant	J·s
J_F	Fowler-Nordheim leakage current density	A/m^2
J_{Ts}	Thermionic emission reverse saturation leakage current density	A/cm^2
k_B	Boltzman's constant	J/°K
L	Transistor channel length	cm
l	TEM camera focal length	cm
λ	Wavelength of an electron	Å
m	Carrier (electron) effective mass	Kg

N_D	Donor concentration of AlGaAs region	cm^{-3}
NF	Noise Figure	dB
n	Number of data points used to measure R_c	-
n_s	2DEG sheet carrier density	cm^{-2}
Q	Charge enclosed by surface area A	Coul
q	Fundamental unit of charge	Coul
R_c	Specific contact resistance (scaled)	$\Omega \cdot mm$
R_{cs}	Large signal source contact resistance	$\Omega \cdot mm$
R_s	Sheet resistance	$\Omega/\blacksquare$
r	Radius of a spot or ring (TEM diffraction)	cm
ρ	Coefficient of linear correlation	-
T	Absolute temperature	°K
V_T	Threshold voltage	V
V_{Th}	Mean (average) measured threshold voltage	V
υ_{avg}	Average carrier velocity	cm/sec
υ_s	Carrier saturation velocity	cm/sec
χ_1	Electron affinity of a small band gap semiconductor	V
χ_2	Electron affinity of a large band gap semiconductor	V
x	Unit vector in direction of x axis	cm
x	Mole fraction of aluminum in $Al_xGa_{1-x}As$	-
y	Unit vector in direction of y axis	cm
y	Mole fraction of indium in $In_yGa_{1-y}As$	-
z	Unit vector in direction of z axis	cm

Abstract

The idea of a new type of Semiconductor Insulator Semiconductor Field Effect Transistor (SISFET) device has been investigated. The attempted design consists of a heavily doped n-type InAs gate with undoped $Al_{0.5}Ga_{0.5}As$ as the gate insulator and with undoped $In_{0.15}Ga_{0.85}As$ as a strained-channel on an undoped GaAs buffer layer. SISFETs provide freedom from the Donor compleX (DX) center and have threshold voltages which are independent of the AlGaAs doping and thickness. Calculations predict that the proposed pseudomorphic structure would produce a device with a natural threshold voltage of approximately 0.6 volts. This would be well suited to digital logic applications. Calculations also predict that this new material structure would provide a barrier to gate leakage of greater than 0.3 volts up to 2.5 volts of positive gate bias. The layers were grown by MBE, and "devices" were fabricated using a self-aligned process which involved ion implantation and rapid thermal annealing. Some finished samples exhibited transistor action, but problems included inordinately high gate leakage and non-ohmic source and drain contacts. Specific contact resistance of 0.65 $\Omega \cdot mm$ was achieved, but the pseudomorphic SISFET was not successfully fabricated as expected. A TEM analysis, along with other electrical and qualitative analyses, support the conclusion that at least one of the problems was the MBE growth.

INVESTIGATION OF A SELF-ALIGNED, STRAINED-CHANNEL, n^+-InAs/$Al_{0.5}Ga_{0.5}As$/$In_{0.15}Ga_{0.85}As$ SEMICONDUCTOR INSULATOR SEMICONDUCTOR FET (SISFET)

I. Introduction

Motivation

The United States Air Force has an interest in developing the technology of Monolithic Microwave Integrated Circuits (MMIC). One specific example of the need for this technology would be the next generation of airborne phased array radar systems [34]. The development of MMIC requires, among other things, high performance microwave amplifiers. A critical part in an amplifier circuit is the high-frequency, low-noise transistor. The low-noise performance produces a higher mean signal-to-noise ratio, and the result is a device that can detect weaker signals from aircraft and satellites. This could translate into the ability to transmit military communications at levels that are more difficult for the enemy to intercept. Furthermore, the military has an interest in the technology of computers. A typical application for the microwave transistor is high speed switching for use in either logic or memory circuits. Heterojunction microwave transistors have recently shown much promise for these applications. However, as the following sections will show,

these transistors also have their shortcomings. A general goal of the research community is to develop a better heterojunction microwave transistor device. This study does not accomplish that monumental goal, but it provides useful results toward that end [34].

Background

As a result of the pursuit for better performance in radars and computers, and thus for higher-frequency and lower-noise transistors, an interesting and active research area is the fabrication of devices based on superlattice hetero-structures. The subject of this thesis effort, which is called a Semiconductor Insulator Semiconductor Field-Effect Transistor (SISFET), is one such device. A similar and better understood device (which will be shown later in Figure 5) is the MOdulation-Doped FET or MODFET. In 1980, J. Rosenburg proposed to replace the metal Schottky-barrier electrode of the MODFET with n^+-GaAs and to eliminate the doping in the AlGaAs [54:379]. This structure (which will be shown later in Figure 2) is called a SISFET. Although little work has been done on the SISFET, the MODFET has exhibited record-breaking performance. When used as an invertor in logic circuits, it has a propagation delay of 12 pico-seconds at room temperature, compared to 2 nano-seconds for a typical MOSFET. The MODFET is also known as: the High Electron Mobility Transistor (HEMT), the Two-dimensional Electron Gas FET (TEGFET), and the Selectively Doped Heterojunction

Transistor (SDHT). The strained-channel or Pseudomorphic MODFET (PMODFET) was first demonstrated by Morkoç and coworkers at the University of Illinois. A 0.25 μm gate length version of this device was subsequently demonstrated to have a maximum frequency of oscillation, f_{max}, of 230 GHz [43;58].

MODFET. This device exhibits an extraordinarily high mobility at low temperatures, resulting in short transit times at low voltages [43;44]. Thus, the MODFET achieves the desirable objective of higher speed and lower power consumption [44]. A necessary requirement for low voltage operation, related to minimum noise levels, is tight control of the threshold voltage. For example, a power supply voltage of 0.5 V requires the threshold voltage standard deviation to be within 10 mV [54]. A problem with the MODFET is that, like the GaAs MEtal Semiconductor FET (MESFET), the threshold voltage is sensitive to processing.

Threshold Voltage. This parameter represents the main advantage of the SISFET compared to the MODFET. The forward gate bias conduction band diagrams for a SISFET and a MODFET are shown in Figure 1. Assuming that the Fermi energy level at the gate is equal to the conduction band energy in the gate at the gate/AlGaAs heterointerface, and neglecting the variation of the Fermi energy in the channel with applied gate voltage, the threshold voltage is given approximately by:

$$V_T = \phi_1 - \phi_2 - (q \cdot N_D \cdot d)/(2 \cdot \epsilon_{Al}) \qquad (V)$$

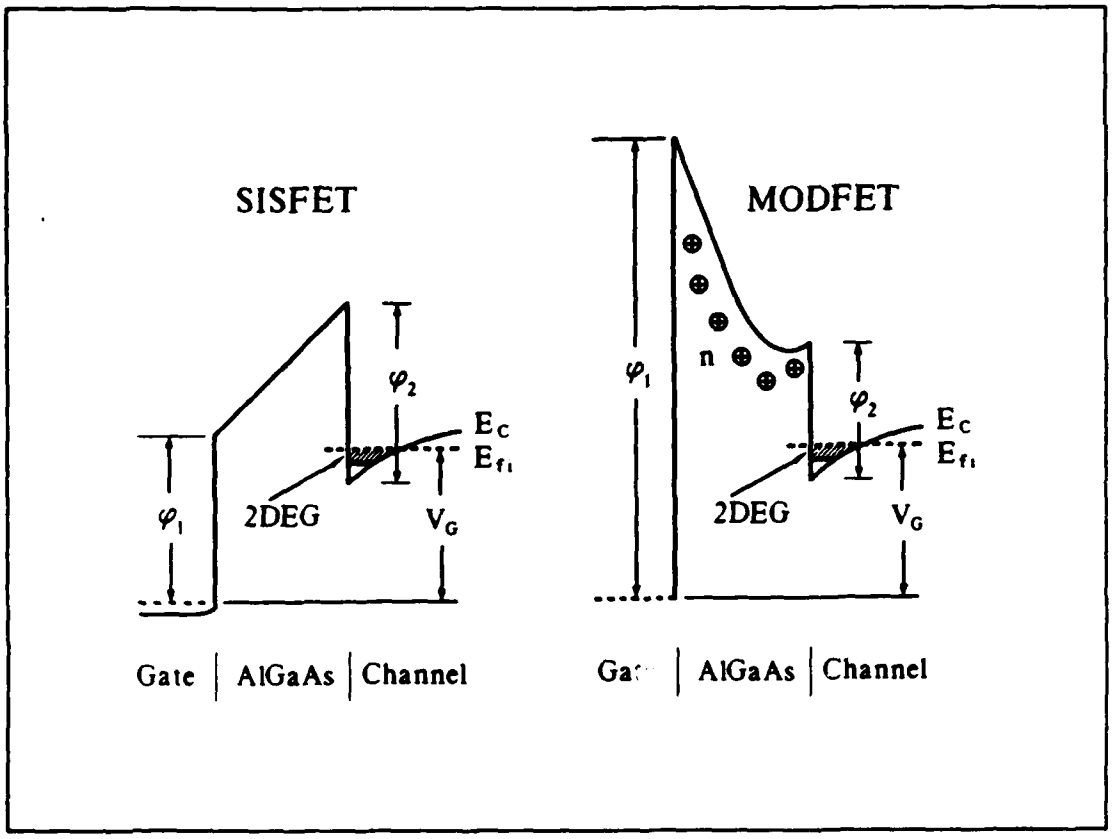


Figure 1. Forward Gate Bias Conduction Band Diagrams for SISFET (left) and MODFET (right) [54:379]

where: ϕ_1 = conduction band discontinuity at the gate/AlGaAs heterointerface (V)

ϕ_2 = conduction band discontinuity at the AlGaAs/channel interface (V)

q = electron charge (coul)

N_D = concentration of donors in AlGaAs barrier layer (cm^{-3})

d = thickness of AlGaAs barrier layer (cm)

ϵ_{Al} = permittivity of AlGaAs barrier layer (F/cm)

The Fermi energy levels for the gate and the channel are indicated by dashed lines. In a MODFET, ϕ_1 represents the Schottky-barrier. The barrier height and ϕ_2 are fixed according to the materials used, but because N_D is large, the value of V_T varies widely depending upon the values of N_D and d. For the standard GaAs gate SISFET, ϕ_1 is a GaAs/AlGaAs heterojunction discontinuity and ϕ_2 is an AlGaAs/GaAs heterojunction discontinuity. The symmetry of the two heterojunctions produces a device with a natural threshold voltage near zero. This occurs because the difference between ϕ_1 and ϕ_2 is small; they are approximately equal.

The key point here is that a SISFET structure results in a threshold voltage which depends only upon the materials used because the AlGaAs is undoped (N_D is three orders of magnitude less). For the MODFET and the SISFET, a more accurate expression for V_T accounts for the variation of the Fermi energy in the channel with applied voltage [46]. The result is derived in Appendix A and is equal to $V_T + E_{fi}$. The device must be in an accumulation mode in order to realize a practically useful conduction. The threshold voltage of the SISFET can also vary from the above expression when ϕ_1 does not equal the barrier height at the gate/AlGaAs interface [48;54]. This is the case if the Fermi energy in the gate region is slightly above the conduction band energy in the gate region at the gate/AlGaAs interface.

Limitations. In addition to the critical dependence of threshold voltage with doping and thickness of the AlGaAs, other disadvantages associated with MODFETs are as follows. Because conduction electrons come from the doped AlGaAs, deep trap states in AlGaAs result in Persistent Photo-Conductivity (PPC) effects and can cause uncontrollable threshold voltage shifts and I-V collapse with changes in either temperature or illumination. Gate voltages larger than the Schottky-barrier height result in parasitic conduction. Also, the hetero-interface may change during high temperature annealing due to field enhanced degradation. There is a electric field (coulombic) interaction between ionized impurities in the AlGaAs and the 2DEG [30;31;17].

The non-self-aligned MODFET has another limitation which arises from the limitations of the fabrication process. In order to create a conduction path to the 2DEG channel, the source and drain contacts are alloyed (diffused) into the channel layer. Further, the fabrication of a depletion mode (normally off) device typically requires recess etching of the AlGaAs layer before applying the Schottky-barrier gate. Both of these factors, combined with the tolerances of the lithography process, limit the performance of the device because they determine channel length. Specifically, the source-to-drain separation results in a channel length on the order of three to four times the gate length. The time required for charge carriers to traverse the channel is not

only a function of their saturated drift velocity, but also of the channel length. A shorter channel length results in faster switching times and a larger forward current gain cutoff frequency which implies a larger f_{max} [34;23].

SISFET. Although the structure of the SISFET is like that of the MODFET, the first obvious difference is that the AlGaAs layer is undoped. As such, the "doping layer" is now simply a barrier layer [27]. Since the undoped barrier layer is much like an insulator, and the conduction electrons are confined to the heterointerface, the SISFET is even more similar to the Metal Insulator Semiconductor FET (MISFET), so widely used in the VLSI industry. Furthermore, the resemblance of the SISFET to a MISFET is even closer with the fact that the gate contact is an ohmic contact to a small bandgap semiconductor. Figure 2 shows a GaAs/AlGaAs/GaAs SISFET structure. This device has been successfully fabricated [42]. The self-aligned structure of a SISFET resulting from ion-implantation creates a channel length which is equal to the gate length. Thus, assuming equivalent electrical properties, the self-aligned SISFET structure is inherently better than a non-self-aligned MODFET structure because of the SISFETs shorter channel length.

In addition to the self-aligned feature of the device, the potential advantages of the SISFET include: 1) the threshold voltage will not be a sensitive function of the doping concentration and thickness of the barrier layer,

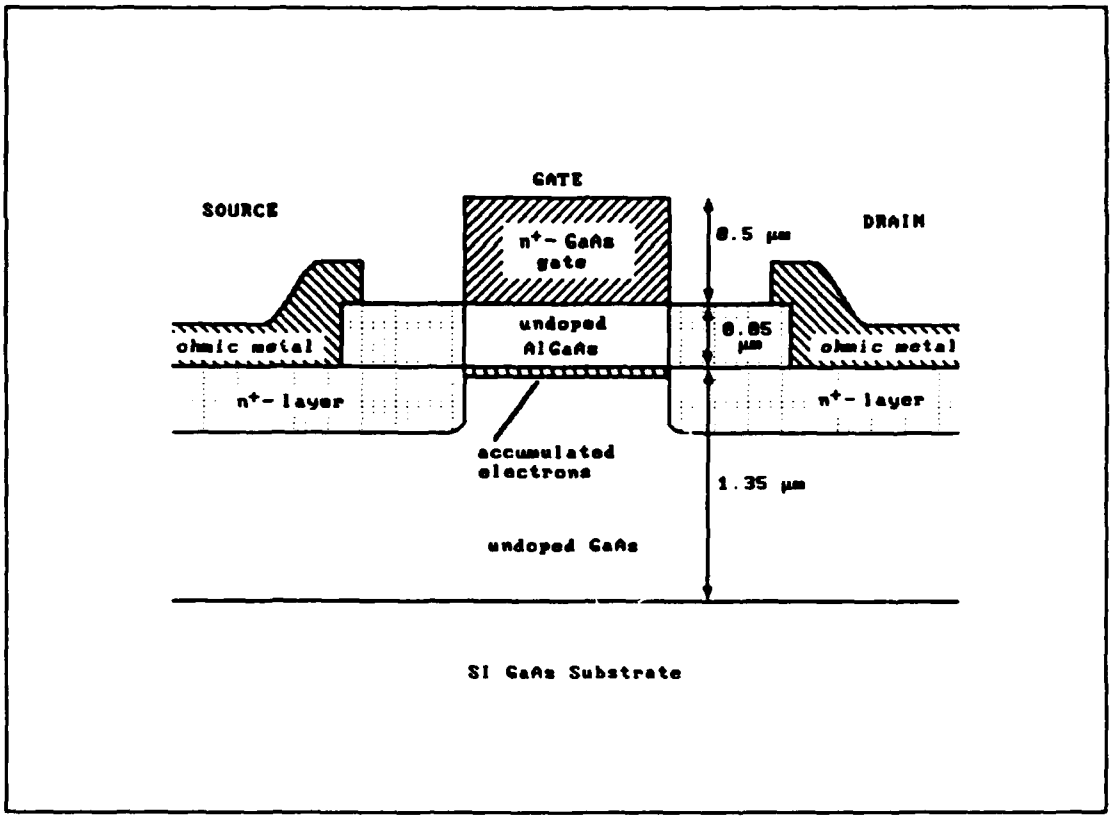


Figure 2. A GaAs/AlGaAs/GaAs SISFET Structure [42:462]

2) the I-V collapse associated with the Donor compleX (DX) trap center will disappear, 3) the gate will support larger gate voltages, and 4) the undoped structure will be more resistant to high temperature annealing [25;54]. Furthermore, since PPC effects will be avoided, the AlAs mole fraction can be as large as possible (for good quality layers) to maximize the conduction band discontinuity and obtain an improved carrier confinement. Chapter II explains in greater detail the structure and operation of the SISFET and how it solves the aforementioned problems of the MODFET.

Problem Statement

Three problems associated with MODFETs include: 1) the threshold voltage is critically dependent upon the doping and thickness of the AlGaAs, 2) gate voltages higher than the Schottky-barrier height result in parasitic conduction, and 3) the channel length is equal to the source to drain contact separation. The objective of this thesis effort was to investigate the fabrication of, and if successful, test a new pseudomorphic or strained-channel SISFET device in which: 1) the threshold voltage is not a sensitive function of the doping and thickness of the barrier layer, 2) the gate supports larger gate voltages, and 3) the channel length equals the gate length. Furthermore, such a SISFET structure would retain the advantages of the pseudomorphic MODFET. Specifically the higher saturation velocities [24], the higher electron mobilities, and the improved carrier confinement in the quantum potential well would still exist.

Scope

The purpose of this thesis was to investigate the fabrication of a self-aligned gate and ion-implanted source and drain, pseudomorphic, n^+-InAs/Undoped $Al_{0.5}Ga_{0.5}As$/Undoped $In_{0.15}Ga_{0.85}As$ heterostructure, Semiconductor Insulator Semiconductor Field-Effect Transistor (SISFET). The design was in concert with recommendations from previous MODFET research [41;35;50] and, the thesis included fabricating the

SISFET depicted in Figure 3. The test program included attempting to measure the DC I-V characteristics, and the specific contact resistance (R_c). The study involved deriving a first-order charge control model for the SISFET structure, and this is included because it provides the theoretical motivation to build the pseudomorphic SISFET. Microwave measurements such as the current gain frequency (f_t), the maximum frequency of oscillation (f_{max}), and the noise figure (NF) were beyond the scope. The study analyzed the measured DC figures of merit, and because the test devices did not operate properly, explanations for device failure were formulated. The failure is reconciled with the results from the verification-type tests and with similar reports from the literature. No improvement over the "proof of concept" design presented in Figure 3 was attempted.

Summary of Current Knowledge

The proposed SISFET structure was an attempt at solving the above mentioned problems by not doping the AlGaAs layer, but instead by doping the source and drain regions via ion implantation. The so called "doping layer" is simply a barrier layer [27]. It was expected that charge carriers would diffuse laterally (primarily from the source and drain regions) into the quantum potential well to create the 2-Dimensional Electron Gas (2DEG) channel [27:381]. Because the barrier layer is undoped, the threshold voltage of such a structure is not critically dependent on the doping and

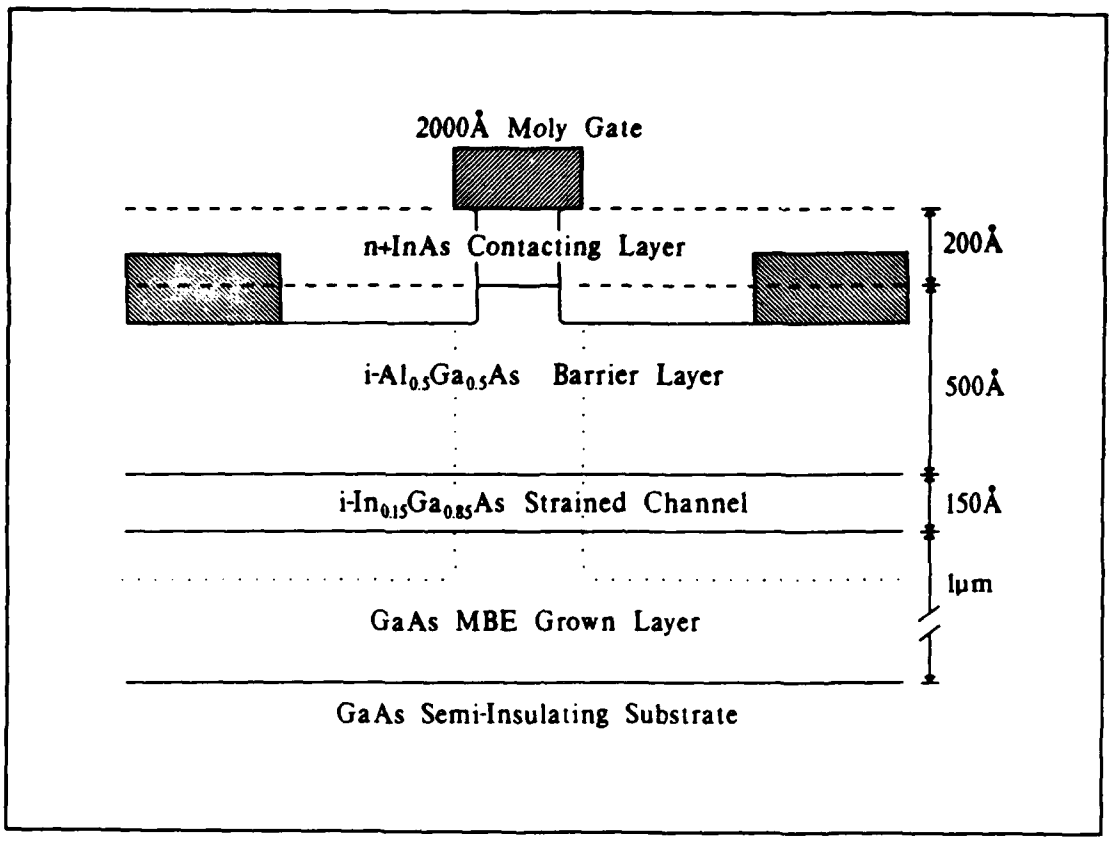


Figure 3. Proposed Pseudomorphic SISFET Structure [41;35]

thickness of the AlGaAs. Instead, V_T is given approximately by the difference in the barrier heights of the InAs/AlGaAs and AlGaAs/InGaAs interfaces [54:379].

An examination of the literature indicates the potential validity of this approach. At least three groups have successfully fabricated self-aligned gate and ion implanted source and drain, heterostructure, lattice matched SISFETs of either n^+-InGaAs/InAlAs/InGaAs on InP or n^+-GaAs/AlGaAs/GaAs on GaAs [15;16;42;54]. In the n^+-GaAs gate (standard) SISFET, the fabricated transistors exhibited a mean threshold voltage

of 35 mV with a standard deviation of 13 mV. The fabrication and analysis of standard SISFETs indicates an increased problem with gate leakage current due to the absence of a Schottky-barrier in this device. However, it was concluded that such structures do, in fact, have the prescribed advantages over MODFETs. PPC effects were not observed, and gate voltages ranged from -4 Volts to +1.4 Volts [54].

The increase of trap states with high AlAs mole fractions and the occurrence of PPC effects are avoided with the SISFET because the charge carriers come from source and drain, not from the AlGaAs. The SISFET is more resistant to high temperature annealing because the concentration of ionized donors in the AlGaAs is from background impurities only. Thus, the electric field perpendicular to the heterointerface is weaker. Also, when the source and drain contacts for a MODFET are alloyed, the AlGaAs surface is exposed. This can result in contamination of the active region (AlGaAs) before the gate is applied. With SISFETs, an advantage is that during annealing and alloying, the gate has already been patterned and so the active region is capped.

Two more subtle advantages have not been mentioned. First, the active region is grown <u>in-situ</u>, eliminating the possibility of any contamination associated with a free AlGaAs surface and the Schottky-barrier gate. Second, parasitic conduction does not occur at large forward gate bias. In fact, any electron entering the AlGaAs is swept into the gate

by the gate field. Thus, less charge is stored in this device meaning that higher transconductance should result. For this effort, it was anticipated that the superior properties of: the higher saturation velocity and mobility in the InGaAs pseudomorphic channel [24], the higher mole fraction of AlAs, and the lower implantation energies would result in a preferred SISFET device. Additionally, the thinness of the InGaAs channel should contribute to higher transconductance.

Approach

The effort included fabricating the SISFET in accordance with established procedures at the University of Illinois and the Air Force Avionics Laboratory. Substrate epitaxial layers were grown by Molecular Beam Epitaxy (MBE). The top n^+-InAs layer was chosen to achieve a low resistance gate contact [47]. Variable sized molybdenum gates 2000 Å thick were deposited in lengths of 2, 4, 6, 10, and 50 μm. The purpose was to provide good statistical projection of measured values. After evaporation of the gates, a self-aligned etch of the capping layer was accomplished. The removal of this cap layer is illustrated in Figure 3.

Calibration of the implantation process was done by implanting ^{+28}Si into MBE grown GaAs samples, annealing, and performing SIMS and C-V measurements. From these results and a consideration of the thicknesses of the MBE layers, the dose and energy to achieve the desired doping profile were determined. The various samples were then subjected to ^{+28}Si

ion implantation to a depth of approximately 750 Å (into the channel layer). The samples were processed with a rapid transit anneal to activate the implant and minimize dopant diffusion. Device isolation was accomplished with a mesa etch to the GaAs substrate. Source and drain contacts were deposited as 400 Å thick AuGe, 100 Å thick Ni, 600 Å thick Al and alloyed (diffused) through to the InGaAs channel layer [42;54].

The DC I-V characteristics and the specific contact resistance were measured when possible. In some cases, the electrical characteristics were so inconsistent that it was not possible to measure meaningful data. Because none of the six fabrication runs produced transistors that worked as expected, every attempt was made to introduce control samples and tests that would uncover problems in the fabrication process. One example of this effort was a TEM analysis of the MBE material before any processing.

The thesis involved developing a classical, first-order charge control model for the new structure. The development of this model was an important part of this effort, and although the predictions remain theoretical, the results from the charge control model are exciting and should continue to motivate further research. Therefore, the details of the derivations and calculations are included in Appendices A and B. The model is unique in that it accounts for the wide variation of the Fermi energy level in the InGaAs over the

range from the flatband condition to strong forward bias (accumulation mode) [48:1017].

Major Results

This thesis effort investigated a completely new kind of SISFET device. A first order charge control model was developed for this structure. The unique aspect of the operation of the pseudomorphic SISFET is that it is an accumulation mode device. The model was extended to provide estimates for threshold voltage, the barrier to gate leakage, and I-V characteristics. These derivations and calculations provided the theoretical motivation behind this attempt to fabricate a pseudomorphic SISFET. A significant result from the calculations is that the proposed pseudomorphic structure would have a barrier to perpendicular transport (leakage) that is two to three times larger than in the standard SISFET. Thus, it is predicted that such a structure might support gate voltages of up to three volts of forward bias. In fact, the calculations show that the sheet carrier density would not reach 5×10^{11} cm^{-2} until one volt of forward bias is applied.

The attempts to fabricate this device proved to be a challenging experience. Transistor action was achieved, but the devices only conducted micro-amperes of current. One significant problem was faulty MBE growth. The variety of different materials in this device made the controllability of the cap layer etch a challenge. There were problems with controllability as well as undercutting. Because this device

is pseudomorphic, shallow implants are the only way to have the peak of the implant contact the channel. There may be a serious problem with channeling of low energy implants at high doses even if the sample is tilted off normal to the (100) plane [34]. This effect may be due to an ion beam defocusing problem. Furthermore, there may be a fundamental problem with implanting into a pseudomorphic heterostructure, particularly where the critical thickness of the AlGaAs is exceeded. Dislocation induced diffusion of impurities may result during high temperature annealing and cause inadvertent doping of the barrier layer [34]. Nevertheless, the potential that this new device promises should continue to be explored.

Plan of Development

The sequence of presentation for this thesis follows. Chapter II reviews the literature pertaining to hetero-structure transistor devices and their principles of operation, particularly with regard to the pseudomorphic or strained-channel heterostructure. This review includes information pertaining to the SISFET structures that have been successfully fabricated and their advantages and disadvantages. Also presented is the result from quantum mechanics which predicts the quantization of electron energy in the channel. The review concludes with a concise description of how the proposed pseudomorphic SISFET will solve the problem. Chapter III details the experimental procedure defined in this study. It provides a description

of any equipment used to either fabricate or test the devices. This chapter further gives the process and the detailed steps of the fabrication of the devices. Chapter IV presents the test configurations, the results, and an analysis of the results in light of the experimental procedure. Given that the test devices did not work as expected, the results are analyzed with respect to the fabrication procedure. The final chapter provides conclusions drawn from the research and gives recommendations for follow-on work.

II. Heterojunction Field-Effect Transistors

Purpose

This chapter reviews current literature pertaining to the structure and basic principles of a self-aligned, strained-channel SISFET. The purpose is two-fold. First, it is to document the current state of knowledge with respect to SISFETs. Second, it is to provide an unfamiliar reader with the background required to understand and appreciate the results of this study.

Overview

The MODFET is a heterostructure device which is similar to the SISFET. Therefore, a logical starting point in this chapter is the operation and fabrication of the standard MODFET. After presenting this technology, along with its drawbacks, this review examines the characteristics of the Pseudomorphic MODFET (PMODFET) and reviews the effect of strain on the electrical properties of such a device. This provides a basis upon which to discuss heterostructure devices in general; their theory of operation, the strained quantum well heterostructure, and the donor complex trap. The strained-channel or pseudomorphic SISFET device attempted in this study has not, to date, been successfully fabricated; however, several groups [15;42;54] have successfully built similar (lattice matched) SISFETs. The results of these efforts is presented in detail. A summary of the major

advantages and disadvantages of the SISFET, as observed from the performance of SISFETs follows. A description of the design of the pseudomorphic SISFET and how it solves the stated problems concludes the chapter.

MODFET

The MODFET, like a MEtal-Semiconductor FET (MESFET), consists of two ohmic contacts (source and drain) and a Schottky-barrier gate which modulates the flow of current between the source and drain. Figure 4 shows a typical MESFET structure with a three-dimensional (or bulk) GaAs channel. High frequency operation in a MESFET requires small gate lengths, but with the smaller dimensions, adequate current carrying capacity requires higher doping concentrations in the channel. In bulk semiconductors, the greater the doping concentration, the lower the charge carrier mobility due to increased impurity scattering [53]. In short, speed versus current capacity is a design tradeoff [12:773].

Operation. Generally, in doped bulk semiconductors, carrier mobility decreases with decreasing temperature because of impurity scattering. At high enough doping levels, impurity scattering will degrade mobility even at room temperature. However, in modulation-doped heterostructures, the designer can meet the requirement for large carrier concentrations in very thin films without the problem of impurity scattering becoming dominant [45:192]. Specifically, in a standard MODFET, as shown in Figure 5, a heterojunction

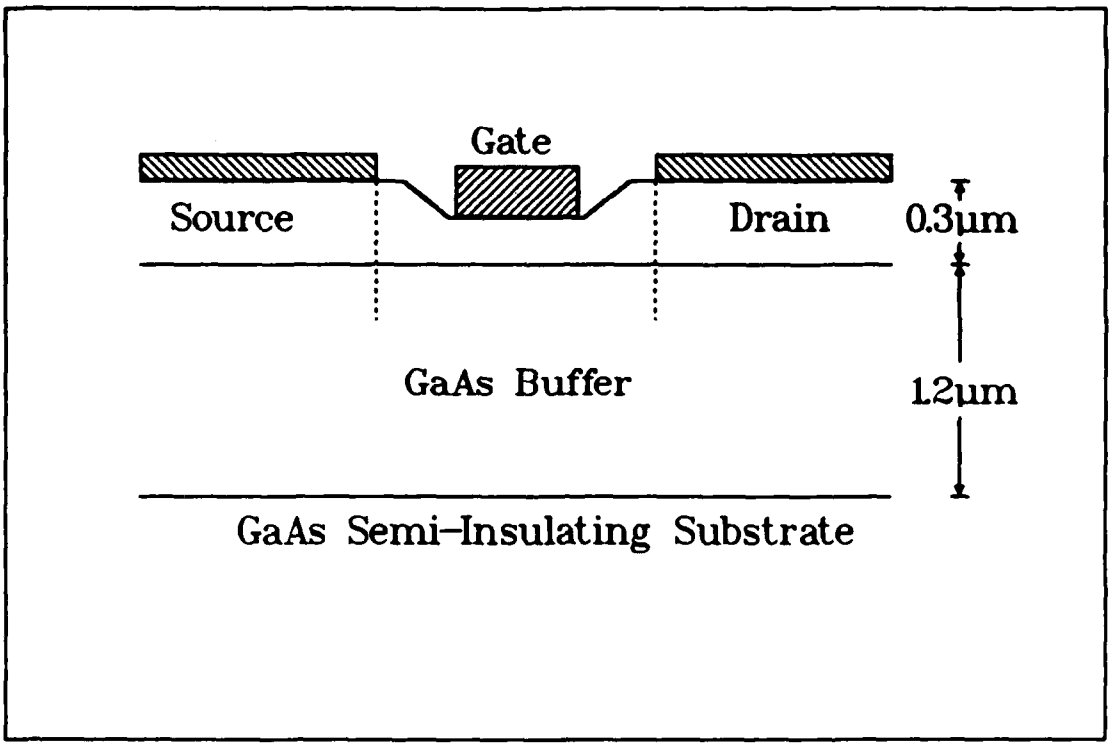


Figure 4. A Typical MESFET Structure. Dotted Lines Indicate Alloying to Produce an Ohmic Contact [3:1399]

consists of AlGaAs and GaAs layers. The structure produces a conduction band discontinuity which results in a quantum potential well that traps electrons at the interface. Electrons from the doped AlGaAs barrier layer diffuse through the undoped AlGaAs separation layer into the lower energy quantum well in the smaller bandgap GaAs layer. The electrons are confined to moving parallel to the interface between the AlGaAs and GaAs [12;44:187]. Current conduction occurs in the undoped region of GaAs. The electron energy is quantized, and the electrons are confined to a thin sheet of charge called

a quasi 2-Dimensional Electron Gas (2DEG) channel [10:790;27]. The spatial separation of the electrons in the GaAs from the ionized donors in the n-doped AlGaAs greatly reduces impurity scattering. The dotted lines indicate the alloying of source and drain contacts in order to obtain an ohmic contact to the channel. The end result is a transistor with high mobilities, large electron velocities, and very large transconductances at very small values of drain voltage [55:1015].

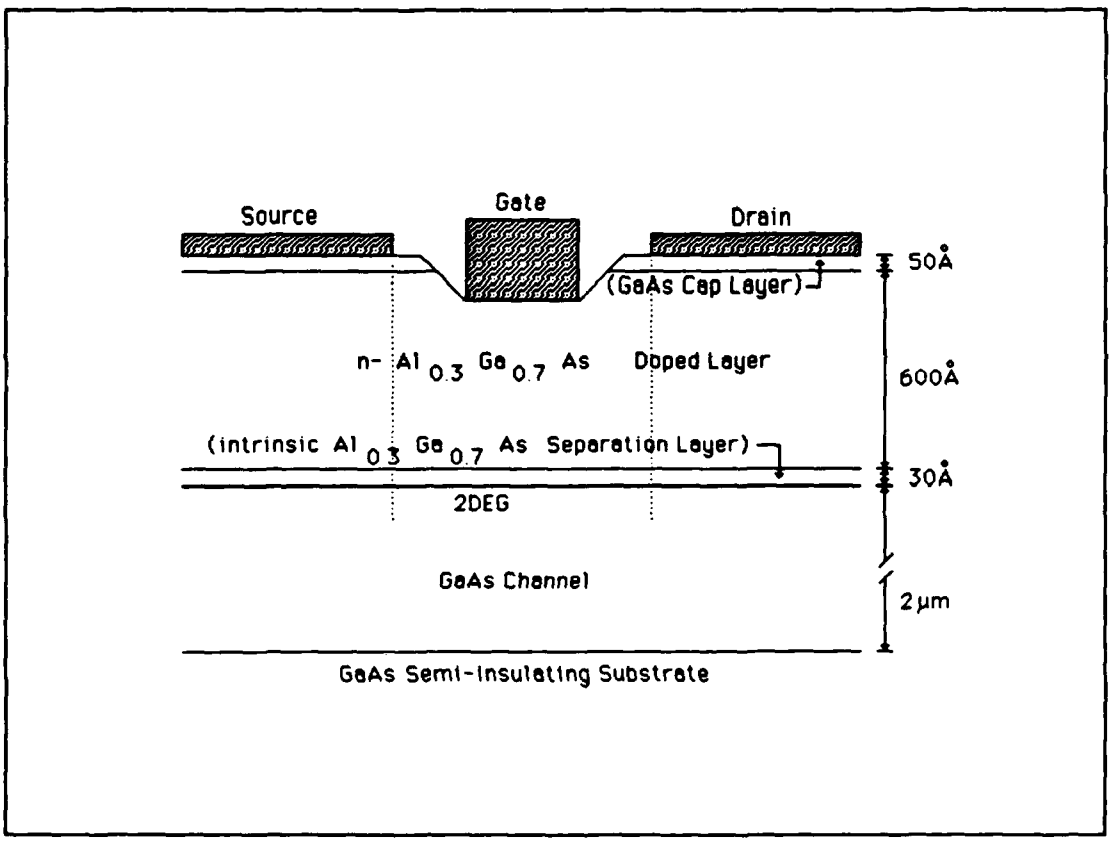


Figure 5. A Typical MODFET Structure [55:1018]

Fabrication. The MODFET fabrication process requires Molecular Beam Epitaxy (MBE) in order to produce thin epitaxial layers with abrupt heterojunctions and doping profiles [37]. Once the buffer, separation, and doping layers are grown on a chromium doped Semi-Insulating (SI) substrate, device isolation is the second step. This involves etching mesas down to the buffer layer. Using either standard electron-beam or optical lithography techniques, the source and drain contacts are defined in positive photoresist. Au, Ge, and Ni are evaporated and a liftoff technique defines the contacts. Annealing or alloying the contacts allows the Ge to diffuse down into the buffer layer and to produce an ohmic contact. The gate region is recessed, and a Schottky barrier gate is applied. The degree to which recessing of the gate is done determines a depletion or enhancement mode of operation [12:792].

Disadvantages. The major drawback of the standard MODFET is its inability to support gate voltages larger than the Schottky barrier height [35]. Thus, the maximum gate voltage is between 0.8-1.0 volts. This is due to: thermionic leakage at the Schottky-barrier gate, tunneling mechanisms at the heterojunction, and a parasitic MESFET conduction path in the n-AlGaAs layer [31:29]. This problem also limits the power capability of the MODFET. One method to improve this disadvantage is to add a thin p+ Be-doped layer between the n-doped AlGaAs layer and the metal gate. This structure is

called an Enhanced Schottky-barrier MODFET (or ESMODFET), but its maximum gate voltage is still limited to 1.6 volts [49;50].

The primary reason for using the AlGaAs/GaAs heterostructure in the MODFET is that the lattice constants of these two materials differ by only a few hundredths of a percent over the entire compositional range of AlGaAs [55:1020]. This allows for growth of heterojunctions that are not dominated by misfit dislocations. However, in practice, the fact that high quality layers of AlGaAs/GaAs may be grown for any AlAs mole fraction is not as important as other considerations. The bandgap of $Al_xGa_{1-x}As$ increases with increasing AlAs mole fraction (x), and in order to have a 2DEG sheet carrier density approximately equal to $10^{12}cm^{-2}$, the conduction band discontinuity ϕ_2 must equal 0.3 volts [35]. This requires a mole fraction of x equal to 0.3. Higher mole fractions would yield a higher 2DEG density, but for x greater than 0.2, problems of Persistent PhotoConductivity (PPC) and uncontrollable threshold voltage shifts dominate. PPC effects cause the collapse of I-V characteristics and are caused by deep level *Donor compleX* trap states (DX centers) in the silicon doped AlGaAs [39:118]. Higher AlGaAs doping increases the 2DEG density, but increases the threshold voltage sensitivity. A final consideration is that the silicon donor binding energy is at a minimum in the range from x = 0.20 to x = 0.30. Thus, the portion $0.25 \leq x \leq 0.30$ of the

compositional range is the most useful for the design of a standard MODFET [35:47].

Pseudomorphic MODFET. A MODFET structure which partially eliminates these problems is called the Pseudomorphic MODFET (or PMODFET). It is also called a strained quantum-well or strained channel MODFET. The PMODFET device is based on an $Al_xGa_{1-x}As/In_yGa_{1-y}As$ heterojunction as shown in Figure 6, where x is the AlAs mole fraction and y is the InAs mole fraction. Because $In_yGa_{1-y}As$ has a smaller bandgap than GaAs, it is possible to achieve the desired conduction band discontinuity with an AlAs mole fraction x equal to 0.15. When x is less than 0.2, PPC effects are greatly reduced [63:84] because the DX center concentration becomes very small. Also, decreasing the AlAs mole fraction permits $Al_xGa_{1-x}As$ to be doped to higher densities due to reduced donor compensation. This feature not only increases the 2DEG density but also causes a slightly larger Schottky-barrier height [55]. Furthermore, a PMODFET has higher saturation velocities, higher mobilities, and improved carrier confinement in the quantum potential well as compared to similar properties of a MODFET [35;38;58].

A major constraint in the use of an AlGaAs/InGaAs heterostructure is a lattice constant mismatch between InGaAs and GaAs. The mismatch increases with a larger InAs mole fraction. For y equal to 0.15 and an InGaAs layer thickness of less than 200 Å, the lattice constant mismatch is approximately 1%. As long as the InGaAs layer is below this

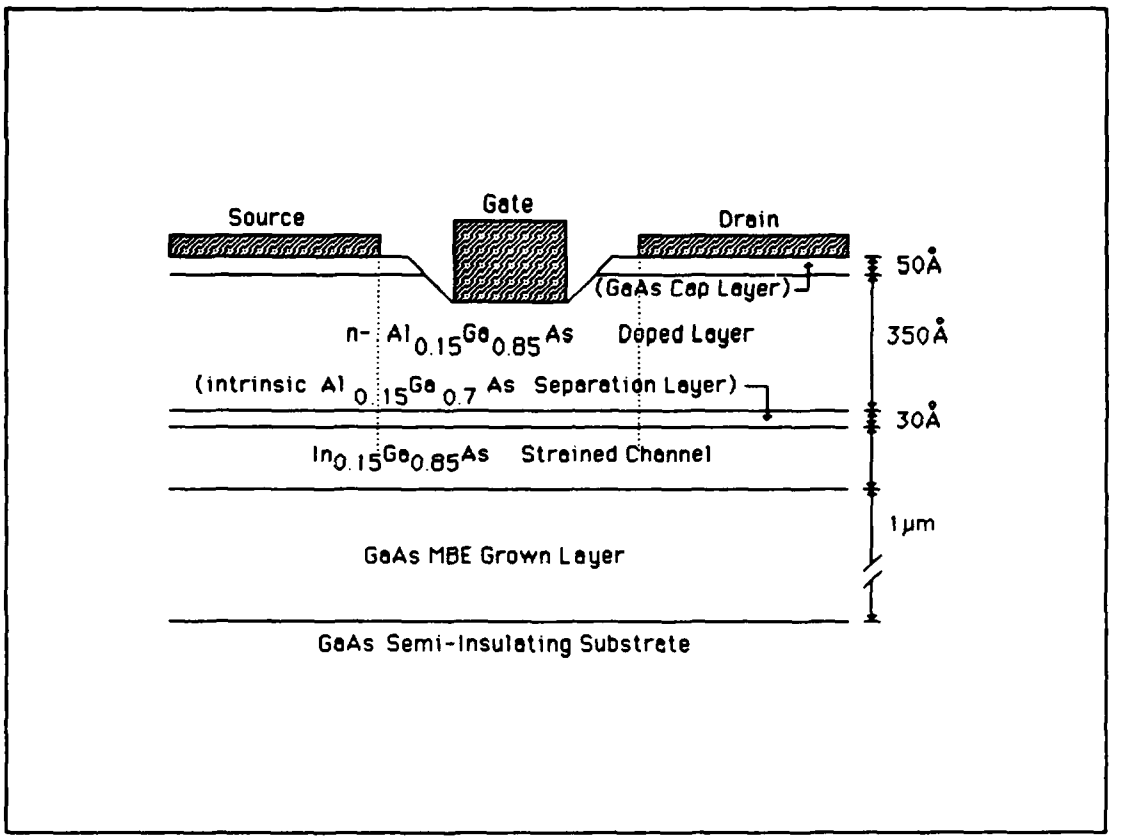


Figure 6. A Pseudomorphic MODFET Structure [38:83]

critical thickness, the layers associated with the hetero-structure are coherently strained. This lattice is called a dislocation free "pseudomorphic" material [63]. The strain results in tension or compression and thus an increase or decrease, respectively, in the equilibrium lattice constant. Figure 7 shows how the energy band gap changes as a function of the equilibrium lattice constant.

Therefore, the strain results in: 1) tension which slightly reduces the energy bandgap of the AlGaAs, and 2) compression which slightly increases the energy bandgap of the

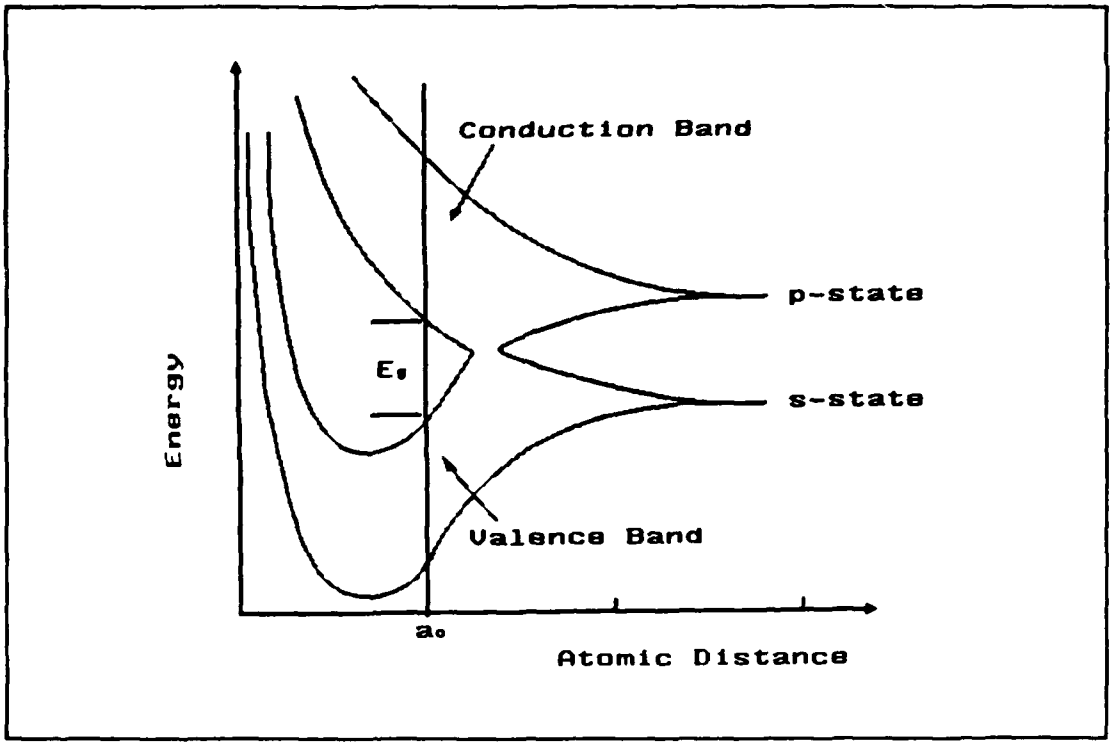


Figure 7. Energy Bandgap as a Function of the Equilibrium Lattice Constant, a_o [63]

InGaAs. The end result is a reduction in ϕ_2, the conduction band discontinuity [39;35]. But overall, PMODFETs have better high frequency performance and lower noise figures [35:50]. Also, it is possible to add a thin p+ layer to increase the Schottky-barrier height to 1.6 volts [52:537;35]. This is called an Enhanced Schottky-barrier PMODFET (or ESPMODFET) [50:6]. Other than the implications of a different and strained material structure, the principles of operation for the PMODFET are the same as for the MODFET. Both devices are quantum well devices. That is to say: the energy of the

conduction electrons, which are trapped in the potential well created by the heterojunction, is quantized. Thus, in order to better understand the principles of operation, it is appropriate to discuss heterostructures.

Heterostructure Devices

A heterostructure simply consists of an abrupt junction between two semiconductors having differing band gap energies [59]. The conduction band and the valence band will be discontinuous at the heterointerface. This situation occurs because the Fermi energy levels align at thermal equilibrium and because the vacuum level must be continuous [40;60]. If the semiconductor having the smaller electron affinity is doped, charge carriers from the impurities will diffuse into (and be trapped in) the quantum well created by the discontinuity [12:776]. With thin epitaxial layers, this well becomes quasi two-dimensional. Thus the name 2DEG. According to Kelly, Anderson's model gives the conduction band discontinuity to be $\Delta E_c = q \cdot (\chi_1 - \chi_2)$ (eV) where χ_1 and χ_2 are the electron affinities of each semiconductor [27:373]. Typically, in a MODFET structure, the conduction band discontinuity is approximately 65 percent of the energy gap difference ΔE_g (eV) [60].

Theory of Operation. The channel layer heterojunction and the resultant conduction band discontinuity (and quantum well) in a MODFET structure are the key to understanding its operation. Indeed, this is the key to understanding any

quantum well device. Fundamental to modelling the MODFET and the SISFET is the estimation of the 2DEG density as a function of the applied gate voltage. The spatial electronic distribution of a mobile electron gas is described, in general, by the Schrödinger (wave function) and Poisson (charge density) equations [53]. When electrons in semiconductors are confined to move within a region surrounded by potential barriers, their energies undergo additional quantization. This occurs when the widths of the potential wells are substantially less than the carrier de Broglie wavelength or electron mean free path. The de Broglie wavelength of a thermal electron is approximately 260 Å at room temperature and becomes longer at lower temperatures [11:338].

Quantum wells are most easily described in one dimension. The analytical solution to Schrödinger's wave equation is based on the assumption of an infinite barrier at the heterointerface and on the linear approximation of the potential in the channel as a function of the perpendicular (surface) electric field in the vicinity of the heterointerface [57:840]. The result is the well known Airy equation [53:519;57]. The sub-band energies with respect to the conduction band in the channel at the heterointerface are given by this equation as:

$$E_n \approx (\hbar^2/2 \cdot q \cdot m)^{1/3}[-3 \cdot \pi \cdot E_z \cdot (n + \tfrac{3}{4})/2]^{2/3} \qquad (V) \quad n=0,1,2,...$$

where: $\hbar$ = reduced Planck constant (J·s)

m = effective mass (Kg)

E_z = surface electric field (V/m) in the channel, derived in Appendix A as $E_z(z=0^-) = -q \cdot n_s/\epsilon_{in}$

This equation approximates the exact solution for the triangular potential well with a 2 percent error [53:519]. The surface field is related to the surface carrier density and ionized impurities in the channel by Gauss' Law.

The density of states is quantized with respect to the ground sub-band, and the first two sub-bands contain 80 percent of the free electrons at room temperature [64:308]. In most device modelling, it is a satisfactory approximation to consider only the first two energy levels. By integrating the product of the density of states function and the Fermi-Dirac statistics distribution, the density of charge in the channel is given by:

$$n_s = \frac{D \cdot k_B \cdot T}{q} \cdot \sum_{n=0}^{n=1} \ln \left[1 + \exp\left[\frac{q \cdot (E_{fi} - E_n)}{k_B \cdot T} \right] \right] \qquad (cm^{-2})$$

where: $D = q \cdot m/(\pi \cdot \hbar^2) = 3.24 \times 10^{13}$ $(cm^{-2} \cdot V^{-1})$

E_{fi} = Fermi energy with respect to the conduction band in the channel at the heterointerface (V)

$k_B = 1.38 \times 10^{-23}$ (J/°K)

T = temperature (°K)

The variable D is the density of states of the 2DEG as calculated from the measured cyclotron effective mass, and k_B is the Boltzmann constant. For the first two energy levels the summation is from n=0 to n=1. Since there are only two relevant levels in the potential well, the discrepancy between the continuous (neglecting quantization in the well) and the discrete models is quite large. Also, because the Fermi energy level is in the quantum well, Fermi-Dirac statistics must be used. As a consequence of these considerations, there is a strong dependence of the Fermi level position on the surface carrier concentration [48]. Motion perpendicular to the interface is hardly affected, and quasi two-dimensional behavior results. A simultaneous solution of the above equation and the one-dimensional Poisson's equation for the potential at the gate yields the value of n_s as a function of the applied gate voltage [57;64]. The equation for electron potential is derived in Appendix A, and the simultaneous solution is accomplished in Appendix B for various values of applied gate voltage.

Strained-Channel. The pseudomorphic or strained-channel heterojunction consists of a quasi-rectangular quantum-well. This well is able to confine the 2DEG more effectively than the quasi-triangular well of the AlGaAs/GaAs heterojunction [44]. This is shown, via the conduction band diagram, for an AlGaAs/InGaAs Pseudomorphic MODFET in Figure 8. The quantum-well layer has gap discontinuities: ϕ_2 equal 0.3 V on the

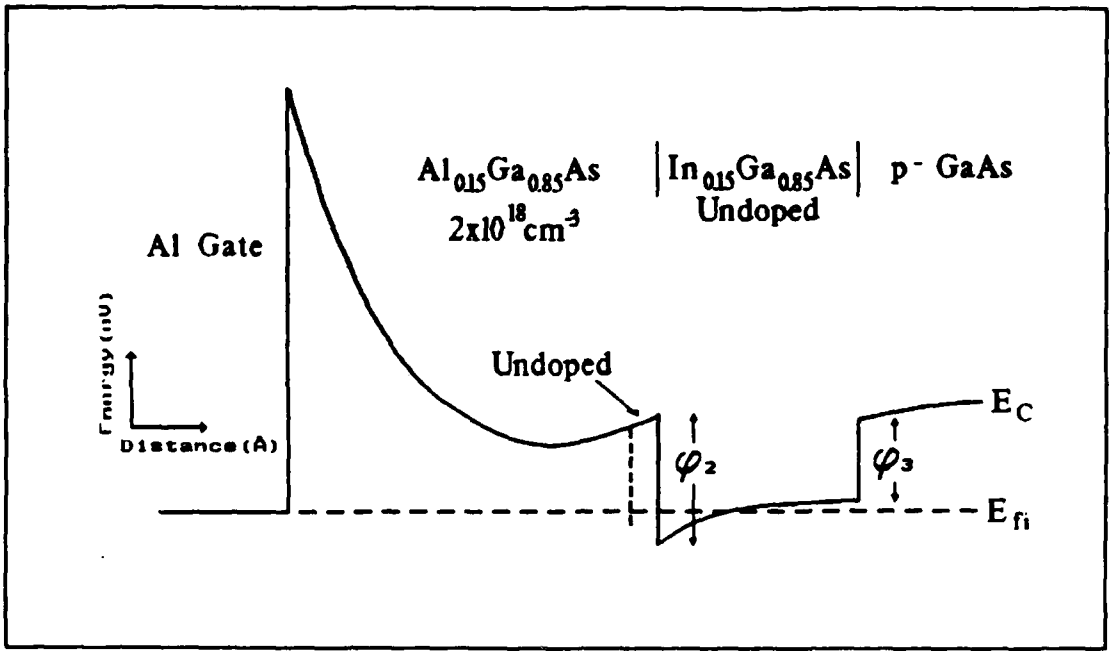


Figure 8. Quasi Rectangular Quantum-Well of a Pseudomorphic Heterostructure MODFET [35:46]

y=0.15 AlGaAs side, and ϕ_3 equal 0.17 V on the p GaAs side. This potential difference forms the quasi-rectangular well. In the standard AlGaAs/GaAs heterostructure, the 2DEG is confined by the barrier $\phi_2 - E_{fi}$ (defined in Chapter I) at the heterojunction. On the GaAs side, the potential barrier results only from the surface electric field. In a pseudomorphic structure, both the AlGaAs/InGaAs and InGaAs/GaAs barrier potentials and this electrostatic potential confine the 2DEG. The result is a higher carrier sheet density n_s for a given gate voltage. This translates to lower output conductance and either greater efficiency or the ability to carry larger currents [35:50].

In a pseudomorphic heterostructure, like the AlGaAs/InGaAs/GaAs system, lattice constant mismatches exist. A plot of energy gap versus lattice constant for several III-V semiconductors is depicted in Figure 9. The lines that connect the points show how the bandgap and lattice constant vary for stoichiometric mixtures of the binary and quaternary (Q) compounds represented by the points. However, if the InGaAs is below a critical thickness, it undergoes a tetragonal distortion (compression) from its normal cubic structure. The epitaxial lattice planes normal to the substrate elongate to produce an atomic plane which is in tension. Because of this feature, the InGaAs is termed a pseudomorphic layer. The importance of this concept is the flexibility it adds to the design process. The designer can use materials such as InGaAs with superior electrical properties for a device channel [63:87]. The main consideration for a strained channel device is that the epitaxial layer with the larger lattice constant be less than a critical thickness [39:118]. For example, given an InAs mole fraction of y=0.15, the InGaAs layer thickness on GaAs must not exceed 200 Å [35:47]. The layer with the smaller lattice constant (typically AlGaAs) above the strained layer (typically InGaAs) will also have a critical thickness.

The strain in these epitaxial layers is depicted in Figure 10, and it results in the modification of the band structure. Under compressive strain, the inter-atomic spacing

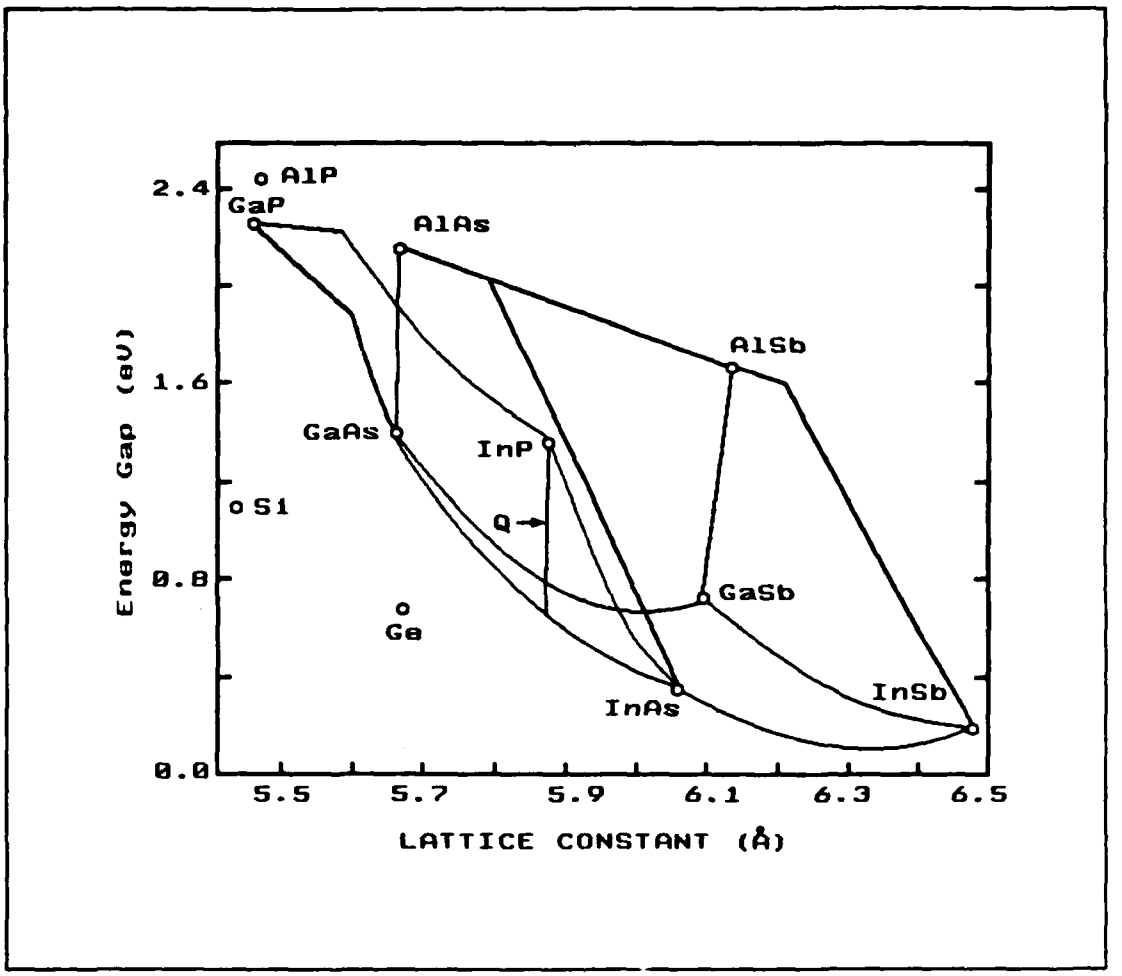


Figure 9. Energy Gap Versus Lattice Constant [35:58]

a_o decreases, and the bandgap increases. Under tensile strain a_o increases, and the bandgap decreases. However, these tensile and compressive strains do not significantly offset the fact that the saturation velocity, v_s, for y=0.15 InGaAs is 33 percent larger than for GaAs [35:47;38]. The larger saturation velocity results in higher intrinsic transconductance, g_{mo}, and an increased forward current-gain cutoff frequency, f_t. This may be shown as follows:

$$f_t = v_{avg}/(2 \cdot \pi \cdot L) \quad (sec^{-1})$$

where L is the channel length (cm) and v_{avg} is the average carrier velocity (cm/sec).

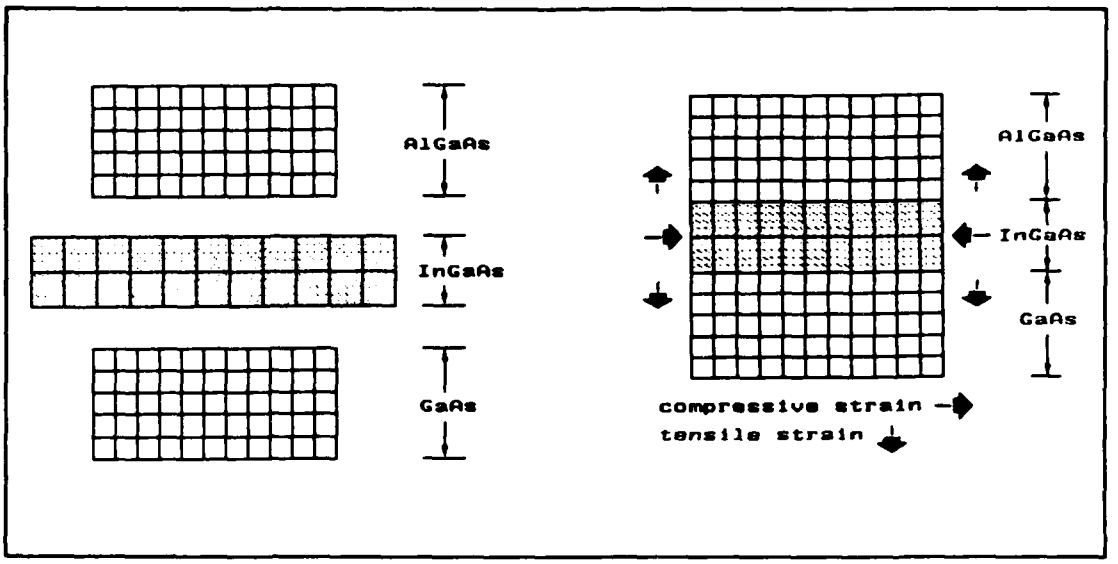


Figure 10. Compressive and Tensile Strain [63:85]

Donor Complex Traps. This serious problem affects heterojunction, quantum well transistors which employ an AlGaAs alloy. These traps manifest themselves in drain current collapse at 77 °K, as well as in threshold voltage shifts and PPC effects. The so called DX center is uniquely associated with n-type AlGaAs, and it has been extensively studied. Some of its properties are as follows. DX centers are associated with AlGaAs donor species. Also, the density of these deep traps approaches the donor concentration and is

increasingly severe for increasing AlAs mole fraction. The density peaks at 40 to 50%. At low temperatures, the DX center is ionized by light. This causes free carriers to remain in the AlGaAs without recapture, and the effect is termed Persistent PhotoConductivity (PPC). These properties are associated with the band structure of AlGaAs [27:380]. A property that is not fully understood is the variation of the silicon donor binding energy with x value. However, it is known that the DX center concentration becomes very small when the AlGaAs is undoped. In undoped AlGaAs, the DX center may be present in concentrations proportional to the number of native defects. The significance of this is that the SISFET is not subject the same I-V collapse of the MODFET. It is because the AlGaAs in the SISFET is undoped.

SISFET

The structure in Figure 2 was an attempt to solve the prescribed problems by not doping the AlGaAs layer but instead by doping the source and drain regions via ion implantation. As such, the previously termed "doping layer" is simply a barrier layer. In a SISFET, the electrons diffuse from the source and drain regions (laterally) into the quantum potential well to create the two dimensional electron gas channel [27:381].

An examination of the literature reveals that SISFETs do operate as stated above [6;26;48;53]. At least three research groups have successfully fabricated self-aligned gate and ion

implanted source and drain, heterostructure FETs of either n^+-GaAs/AlGaAs/GaAs on GaAs or n^+-InGaAs/InAlAs/InGaAs (lattice matched) on InP [15;42;54]. The success that these groups have had in building SISFETs buttressed this effort and the idea that it is possible to build a pseudomorphic SISFET. The following subsections summarize the work of each group.

Matsumoto and Others. This Japanese group (1984) fabricated the first self-aligned accumulation-mode GaAs Metal Insulator Semiconductor (MIS)-like FET having an n^+-GaAs/ undoped AlGaAs/undoped GaAs structure. The devices were named SISFETs. The group tested 41 samples that showed an average threshold voltage, V_{Th}, of 0.035 V with transconductance, g_m, as high as 170 mS/mm for a 2 μm gate length. The n^+-GaAs layer is used as a gate in this structure, and because the AlGaAs layer is undoped, the fabrication process naturally produces a device with a threshold voltage near zero. The structure, which has already been shown in Figure 2, was grown by MBE. It consisted of a 1.35 μm undoped GaAs buffer layer, a 0.05 μm undoped x=0.4 AlGaAs barrier layer, and a 0.5 μm n^+ silicon doped GaAs gate layer. The top n^+ layer was selectively etched to form a gate which also functioned as a mask for ion implantation. The source and drain were implanted with silicon ions at a flux of 2×10^{13} cm^{-2} and an energy of 100 KeV. Rapid annealing was done at 800 °C for 30 seconds. The AlGaAs layer was selectively etched. Finally,

evaporating and alloying the source and drain contacts completed the process [42].

Solomon and Others. This group at IBM (1983) fabricated a SISFET structure of GaAs/AlGaAs/GaAs layers; however, unlike the Matsumoto group, the Solomon group selectively etched all of the AlGaAs when patterning the gate before ion implantation. Additionally, the thicknesses of the respective layers were slightly different. The significance of this study is that they achieved results similar to those of Matsumoto's team. The short channel (1 μm) devices showed threshold voltages within 50 mV of zero and transconductances as high as 240 mS/mm with a normalized (scaled resistance, i.e. multiplied by the contact width) drain resistance of 2 $\Omega \cdot$mm [54]. Typical measured contact resistances, R_c, ranged from 0.1 to 0.3 $\Omega \cdot$mm [53:602].

A schematic cross-section of this SISFET is shown in Figure 11. These structures were grown by MBE on a (100) Semi-Insulating (SI) GaAs substrate. A 1 μm undoped GaAs buffer layer, a 600 Å undoped $Al_{0.4}Ga_{0.6}As$ barrier layer, and a 0.4 μm GaAs n^+ silicon doped capping layer were then grown. Next, a 0.15 μm molybdenum layer was deposited by electron beam evaporation. The molybdenum gate contact is ohmic. The metal was patterned using a reactive ion etching technique (RIE) and a CF_4-O_2 plasma. The GaAs was selectively etched using a CCl_2F_2-He plasma which stops at the AlGaAs surface. This process resulted in some undercutting. Source and drain

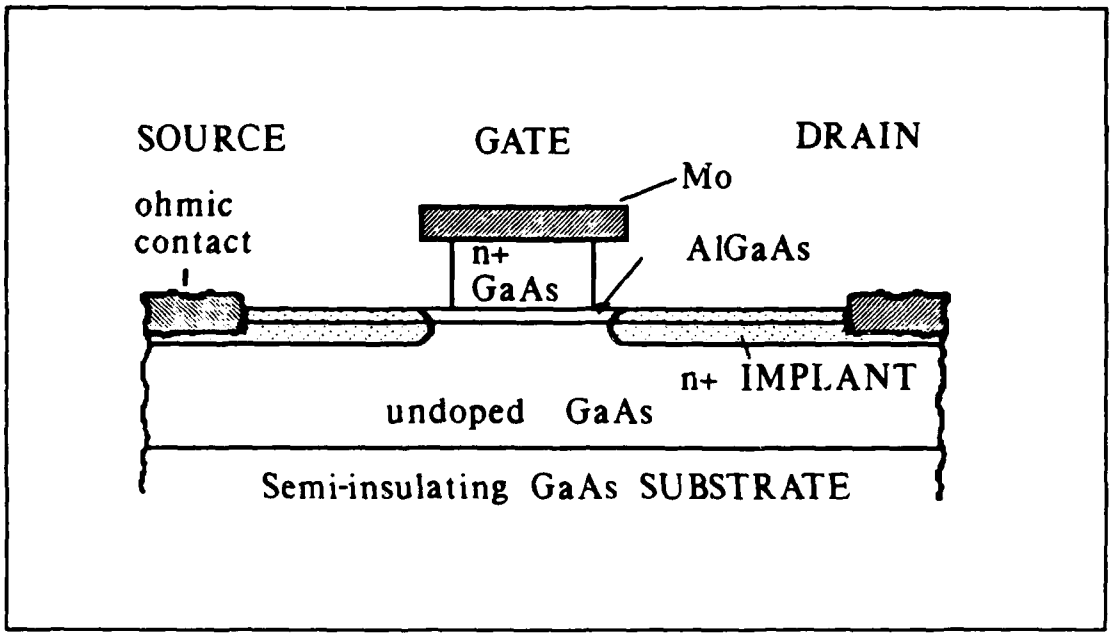


Figure 11. Cross Section of GaAs Gate SISFET [53:601]

regions were then implanted with 100 KeV silicon ions at a dose of 5 x 10^{13} cm^{-2}. The devices were annealed at 750 °C for 2 sec. Finally, Au/Ni/Au-Ge ohmic source and drain contacts were evaporated and alloyed [53].

Feuer and Others. This group at AT&T Bell Laboratories (1987) fabricated lattice matched SISFETs with n^+-InGaAs gates on an InP substrate. The motivation for this study was to take advantage of the superior properties of an InGaAs channel. The structure consisted of a 0.4 μm $In_{0.53}Ga_{0.47}As$ channel layer, a 0.06 μm $In_{0.53}Al_{0.48}As$ barrier layer, and a 0.2 μm n^+-$In_{0.53}Ga_{0.47}As$ gate layer. The fabrication process was similar to the Solomon group, except that different materials were used. One main difference was the implantation of

silicon ions with a dose of 5 x 10^{13} cm^{-2} and an energy of 150 KeV. The sheet resistance of the implanted material, R_s, was 40 Ω/■. The finished devices exhibited a transconductance as high as 250 mS/mm for a 1.7 μm gate length; however, the devices could not be pinched off. They attributed [15:35] this result to parasitic conduction in the channel which is either due to a thick channel or too large an energy for ion implantation [15].

One year later this same team was more successful. These layers were grown on Fe-doped semi-insulating InP substrates. The layers consisted of: a 0.3 μm $In_{0.53}Al_{0.48}As$ buffer layer, a 0.03 μm $In_{0.53}Ga_{0.47}As$ channel layer, a 0.05 μm $In_{0.53}Al_{0.48}As$ barrier layer, a 0.005 μm $In_{0.53}Ga_{0.47}As$ spacer layer, and a 0.2 μm n^+-$In_{0.53}Ga_{0.47}As$ gate layer. First, a 2000 Å gate mask layer of tungsten was deposited as the gate metal, using electron beam evaporation with Ar^+ bombardment to relieve stress. Reactive ion etching in SF_6 and then $CCl_2F_2/He/O_2$ was used to pattern the W gate mask and then etch the n^+ InGaAs cap layer, respectively. Thus, total undercutting was minimized to less than 0.1 μm of the 1.1 μm gate metal length [16:162].

Self-aligned source and drain contacts were implanted at room temperature using ^{+28}Si ions at a dose of 2 x 10^{13} cm^{-2} and at an energy of 150 KeV. Samples were proximity annealed under a GaAs cap for 10 seconds at 750 °C. Next, source and drain contacts of Au/Ge/Ni were deposited and alloyed.

Finally, mesa isolation was accomplished using a wet etch. This etch undercut the gate between the gate contact and the active region. This was done to avoid leakage current at the mesa edge [16:162].

For these devices, the gate lengths were 1.1 μm and gate widths were 100 μm. The devices exhibited sharp pinchoff and low output conductance on the order of 10-20 mS/mm. Forward bias gate leakage was typically 50 μA at +1.0 volts (V_{DS} = 0 volts). Reverse bias leakage was typically 20 μA at -1.0 volts. Peak extrinsic transconductance was 220 mS/mm. Specific contact resistances of source/drain contacts was 2.0 $\Omega \cdot$mm (high) because of contamination. Sheet resistance for the gate contacts was typically 2 $\Omega/\blacksquare$. Microwave measurements revealed a maximum frequency of oscillation, f_{max}, equal to 19 GHz. The unity current-gain cutoff frequency, f_t, was equal to 27 GHz. The dominant factor limiting microwave power gain was attributed to high gate contact resistance [16:162-164].

Performance Summary. The performance of the transistors fabricated by these research groups is summarized in Table 1. In all cases the transistors operated, had high transconductances for the gate lengths involved, and had threshold voltages within 500 mV of zero. The first SISFET on InP had considerable parasitic conduction problems, but the second attempt by Feuer's team produced excellent results. However, work on InP substrates is in its infancy as compared to GaAs.

Table 1. Performance Summary of Successfully Fabricated Lattice Matched SISFETs

		Gate Length (μm)	g_m (mS/mm)	V_{Th} (mV)	R_c ($\Omega \cdot$mm)	R_s ($\Omega/\blacksquare$)
Matsumoto		2	170	+35	-	-
Solomon		1-2	240	+50	0.1-0.3	150
Feuer	a)	1.7	251	-	0.1	40
	b)	1.1	220	-500	2.0	2

		Comments and/or Problems
Matsumoto		Gate voltages to +0.8 volts with less than 40 μA gate leakage
Solomon		Gate voltages ranging from -4.0 to +1.4 volts with less than 10 μA gate leakage
Feuer	a)	Devices could not be pinched off; V_{Th} not measurable
	b)	f_{max} = 19 GHz, f_t = 27 GHz. Gate voltages to +1.0 volts with 50 μA gate leakage

It is less well understood and less prevalent, and GaAs is a physically stronger material. For these reasons, this effort has concentrated on improving SISFET technology on GaAs. Furthermore, it is conceivable that a pseudomorphic SISFET on GaAs could out perform the lattice matched SISFET on InP.

The results of the standard SISFETs on GaAs indicate an increased problem with gate leakage current due to the absence of a Schottky barrier in this device [14;31;56]. However, it was concluded that higher AlAs mole fractions could help this problem to some degree, and that such structures do, in fact, have the following advantages when compared to MODFETs. Threshold voltages are naturally near zero because there is no doping in the barrier layer. Because the barrier layer is undoped, the parasitic MESFET problem is removed. Since charge carriers diffuse laterally from the source and drain regions, trap states (DX centers) in the AlGaAs layer no longer cause the collapse of I-V characteristics at low temperatures. This feature also permits the use of a high AlAs mole fraction in order to increase the conduction band discontinuity and have better confinement in the quantum well. Some sensitivity to light at 77 °K was observed (PPC effects), but nothing like the variations that occur in a MODFET. Also, a broader range of gate voltages were supported. The voltages ranged from -4 to +1.4 volts [42;54].

Work on SISFETs to date has been strictly on the individual device level. One problem with these devices is that undercutting of the gate results in an unimplanted and ungated region. Since the device requires a forward bias to conduct, this region is a built-in series resistance. However, the non-variant threshold property of SISFETs has been verified with a small standard deviation. As summarized

above, transconductance values have been good. The capacitance to g_m ratios indicate carrier velocities greater than 2×10^7 cm/sec which is superior to those of a MODFET. This is attributable to better confinement in the well from the higher x value of the AlGaAs barrier layer. Although self-aligned MODFETs have been reported [5], the MODFET is still limited to an x value less than 0.3. Finally, as far as application to logic or memory circuits, although a zero or slightly negative threshold voltage is not ideal, the threshold voltage could be shifted by lightly doping the barrier or by selecting a different material system [27:381]. The proposed strained-channel SISFET would solve this problem by having a positive threshold of approximately 0.6 Volts (the difference between ϕ_1 and ϕ_2).

Gate Leakage. Because the barrier layer is not a good insulator (as compared to the MISFET), the barrier voltages for the SISFET are low. This creates a problem with gate leakage. Gate leakage is perpendicular transport of charge carriers across the heterojunction barriers. The physical mechanisms for the gate leakage current are thermionic emission and Fowler-Nordheim tunneling. Both currents are exponentially dependent on the barrier height, ϕ_B. For thermionic emission, the reverse bias saturation current density is given by the following [27:376]:

$$J_{TS} = A^* \cdot T^2 \cdot \exp[-\phi_B/(k_B \cdot T/q)] \qquad (A/cm^2)$$

where: A^* = modified Richardson's constant ($A \cdot cm^{-2} \cdot {}^\circ K^{-2}$)

T = absolute temperature (°K)

ϕ_B = barrier to perpendicular carrier transport (gate leakage) as measured from the Fermi energy level = $\phi_2 - E_{fi}$

Thermionic emission occurs when a charge carrier has sufficient kinetic energy imparted to it from the vibration of the lattice that it can move over the potential barrier ϕ_B. For tunneling, since the application of a forward gate bias to the SISFET results in a trapezoidal barrier shape, the Fowler-Nordheim formula applies. The current density is given by [27:377]:

$$J_f = A \cdot F^2 \cdot \exp[{}^4/_3 \cdot (2 \cdot m \cdot q)^{1/2} \cdot \phi_B^{3/2} / (\hbar \cdot F)] \qquad (A/m^2)$$

where: A = constant in terms of effective mass and the barrier height ($\Omega^{-1} \cdot V^{-1}$)

F = applied field (V/m^2)

The maximum barrier height, ϕ_B at zero bias, of the AlGaAs/GaAs SISFET with an x value between 0.4 and 0.6 is on the order of 0.3 volts (as compared to 3 volts for a MISFET). Essentially, this results because undoped AlGaAs is not really a good insulator. Under forward bias conditions, the barrier height is reduced further because of the formation of the quantum channel. This problem seriously limits performance,

and specifically, the maximum operating temperature of the device. An examination of the proposed pseudomorphic structure in Appendix B yields a barrier height on the order of 0.6 volts, even with a +1.0 volt bias. This is a result of the larger band gap of x=0.5 AlGaAs and the smaller band gap of y=0.15 InGaAs. Therefore, in the pseudomorphic SISFET of this study, gate leakage should, in principle, be less of a problem [27:383].

Pseudomorphic SISFET. The conclusion of all three groups was that the SISFET has real potential for application as a low-power consumption, high-speed logic device. With regard to the pseudomorphic SISFET in this effort, the superior properties of the InGaAs channel, the higher mole fraction of AlGaAs, and the lower implantation energies should, in principle, result in not only a better SISFET but potentially a preferred transistor device. Second, the small value for ϕ_1 (resulting from the low band gap n^+-InAs gate), should produce a positive threshold voltage. Third, because the barrier to gate leakage (ϕ_B) is larger, this should be less of a problem. Finally, the thinness of the InGaAs channel should result in a higher transconductance [12:773;15;42]. All of these considerations served as the technical motivation for this research effort.

The final section of this chapter reviews the design of the proposed pseudomorphic SISFET and why it is believed that it solves the problem statement of Chapter I. The idea of the

pseudomorphic SISFET and the proposed design originated with Dr. Hadis Morkoç at the University of Illinois. The scope of this effort was to fabricate and test the proposed structure as given to the author by Dr. Morkoç and as presented in Chapter I. Nevertheless, it is useful to discuss the rationale behind the design. It is worthwhile to document this thought process because it will aid in further research.

A discussion of the material selection and the geometries involved is appropriate. The GaAs buffer layer simply provides for the start of good quality MBE growth. It is also possible in this layer to produce a Strained Layer Superlattice (SLS) structure in order to prepare for the epitaxial growth of the $In_{0.15}Ga_{0.85}As$ layer. The 15% mole fraction of InAs duplicates the structure of a PMODFET so that the 150 Å thickness is below the critical thickness.

The material InGaAs was chosen because this alloy has: a smaller bandgap energy, a larger low field mobility, and a higher saturation velocity than GaAs. The next layer of 50% AlAs mole fraction AlGaAs was chosen because this is the largest mole fraction of AlGaAs that can be grown by MBE with high quality. In the SISFET structure, the AlAs fraction should be maximized because of the large bandgap energy of AlAs compared to GaAs. The larger the bandgap of the better the material acts like and "insulator." In fact, the larger bandgap AlGaAs and the smaller bandgap InGaAs combine to give a large heterojunction conduction band discontinuity. A

larger discontinuity results in a higher barrier to gate leakage and better confinement in the quantum well.

There is also a critical thickness associated with the AlGaAs, and the optimum condition would be to not exceed it. The 500 Å thickness may exceed the critical value, but it was believed that this is acceptable in a barrier type region. Furthermore, the AlGaAs layer needs to be sufficiently thick to have material to implant through to contact the channel. This is so because the cap layer is etched before implantation.

The n^+InAs layer was chosen for two reasons. First, the gate contact in a SISFET must be an ohmic contact. Recent studies have shown that contacts on heavily doped InAs result in some of the lowest reported contact resistances to date [47]. The original intent was to use the InAs to provide low resistance source and drain contacts as well. This would entail etching the cap layer as the last step instead of right after gate deposition. Second, the bandgap of pure InAs is very small. The advantage here is that it produces a device with a positive threshold voltage because the value of ϕ_1 is very large. The thickness of the InAs was set to provide enough to accomplish the low resistance contact but no more.

Lastly, it is appropriate to discuss why the proposed structure should solve the stated problems. First, the threshold voltage of any SISFET structure has already been shown to be insensitive to the doping and thickness of the

AlGaAs. The pseudomorphic SISFET would be no different. Second, the standard SISFET has been shown to support gate voltages to +1.4 volts, which is better than a MODFET. Since the pseudomorphic SISFET would have twice the barrier to gate leakage (the primary drawback of the standard SISFET), this new structure would support higher gate voltages. Third, the ion implantation technique, which uses the gate metal as an implant mask, will result in a self-aligned device.

Furthermore, because of the use of InGaAs as the channel layer, the pseudomorphic SISFET would have the higher saturation velocity, higher mobility, and better quantum well confinement of the pseudomorphic MODFET. The following chapter describes the fabrication process. It describes the method, the equipment, and the specific steps that were taken to fabricate this new and potentially revolutionary device.

III. Experimental Fabrication of the Self-Aligned, Strained-Channel SISFET

Purpose

This chapter presents a description of the process, equipment, and procedures that were used to fabricate and characterize the SISFET structures. A brief overall process description is followed by a functional description of the equipment. Lastly, the device fabrication process and procedures are described in detail.

Process

The fabrication process begins with semi-insulating GaAs wafers. The MBE growth process involves preparing the wafer, accomplishing the growth of the semiconductor layers, cleaving the wafer, removing indium solder, and lapping the individual samples. This results in the material needed to begin the photolithographic steps. At this point, the MBE growth can be verified through the use of SIMS, TEM, Auger, or Photo-luminescence data. The gate deposition process involves evaporating and patterning the molybdenum gates and a wet chemical (self-aligned) etch of the cap layer. After patterning the gates and before etching the cap layer, the ohmic quality of the gate contacts may be evaluated. Taking profile measurements verifies the result of this critical etch step. Ion implantation and annealing involve subjecting the sample(s) to energetic ^{+28}Si ions and rapid heating and

cooling. This results in a self-aligned doping of the regions not covered by gate metal and in electrical activation of the dopant. At this point, the implantation and annealing can be verified through the use of SIMS, C-V, or four-point probe data. The source and drain deposition involves isolating the devices with a mesa etch, evaporating and patterning the source and drain contacts, and alloying the contacts. This completes the device fabrication.

Equipment

The SISFET fabrication process required equipment present at both the Avionics Laboratory (AFWAL/AADR) at Wright-Patterson AFB and the Coordinated Sciences Laboratory (CSL) at the University of Illinois. SISFET structures were grown by MBE and gates evaporated at CSL. Ion implantation and annealing were done at AFWAL, and fabrication was completed at CSL. Testing was done at both AFWAL and CSL.

MBE Growth. The substrates or layers were prepared by graduate students at CSL according to the specifications for this proof of concept structure. The MBE system at CSL is a Riber Model 1000. It is designed for research activities as opposed to a production environment. Epitaxial growth is achieved when thermal, molecular beams of semiconductor and impurity elements impinge on a heated substrate (on the order of 630 °C) in an ultra high vacuum (10^{-11} torr) environment. A schematic of a typical MBE system is shown in Figure 12. Opening and closing effusion cell shutters and varying

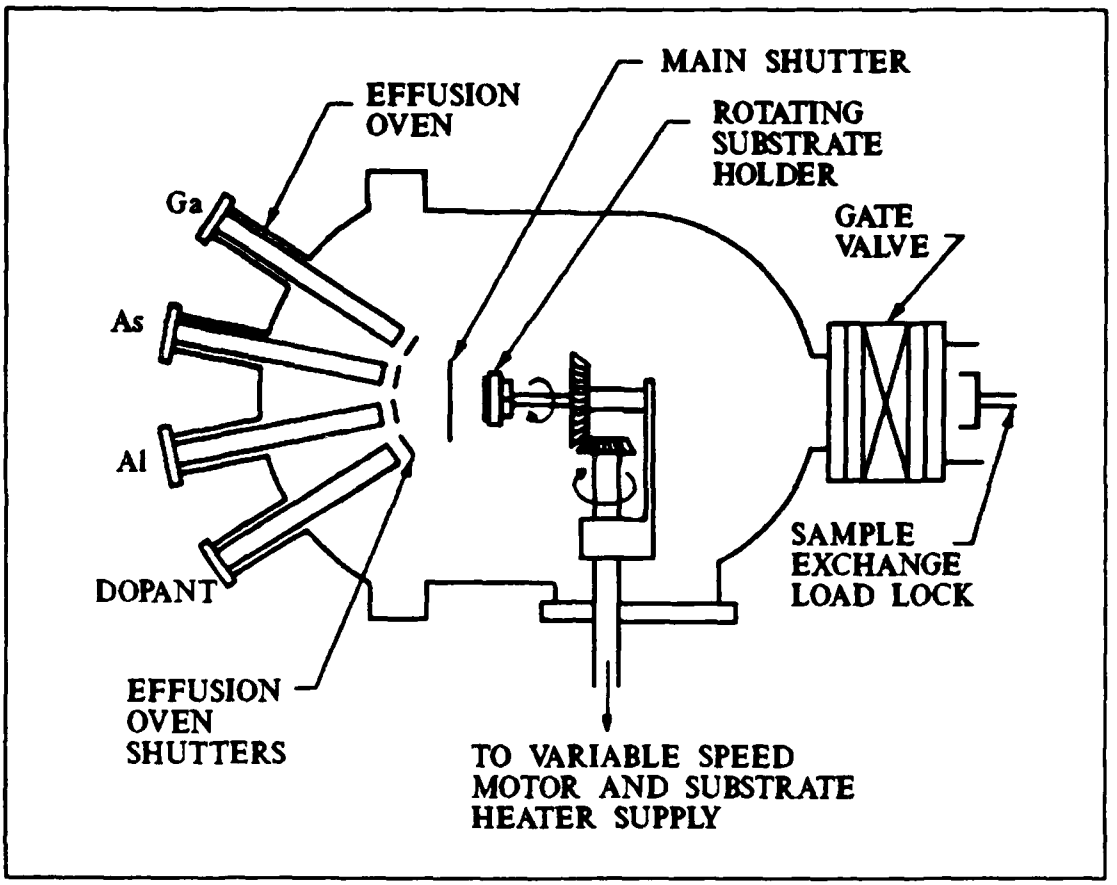


Figure 12. Schematic of a Molecular Beam Epitaxy System [59:337]

effusion cell temperatures controls the growth process. The effusion cells available were: two As cells, a Ga cell, an Al cell, an n-type dopant Si cell, and an In cell. The fluxes produced from each effusion cell are molecular beams whose effusion fluxes are exponentially dependent on cell temperature. The exact dependence is a function of the elemental source, the effusion cell design, and the amount of the elemental material. Therefore, for each effusion source,

it is necessary to monitor the flux density of impinging atoms and to use empirical calibration relationships. This information predictably determines the actual growth rate and dopant concentration. Additionally, electron diffraction patterns are used to provide feedback during the MBE growth process.

Spinner. The spinner used was manufacture by Headway Research, Inc. It has a vacuum chuck to hold the sample and the ability to spin the sample at 5000 rpm. Samples were spun at 5000 rpm for 30 seconds immediately after photoresist was applied.

Ovens. These were used for pre-baking, post-baking, drying, and alloying the samples. They were metal boxes with the temperature controlled by hotplates. Three ovens were operated at a constant 70 °C, 90 °C or 110 °C, respectively. Alloying the source and drain contacts was performed with an electrically heated glass tube which could be purged with nitrogen.

Mask Aligner. The mask aligner used to expose the photoresist was a Karl Süss, model MJB 3HP UV400. The lamp was a 180 Watt mercury vapor lamp. The photoresist was exposed for either 7.5 or 13 seconds depending on the type used. The photoresist process is detailed in the latter part of this chapter. The aligner was capable of printing device geometries (like gate lengths) on the order of 1 μm. The masks used were developed by Dave Look at AFWAL and consisted

of gated and ungated Van der Pauw patterns, Transmission Line Method (TLM) patterns, and transistors with gate lengths ranging from 2 to 50 μm [4]. Figures of the individual masks will be shown later in this chapter. The overall mask pattern used is shown in Figure 13.

Evaporation Chamber. This instrument was used for evaporating both the refractory metal molybdenum gate as well as the AuGe/Ni/Au source and drain contacts. The evaporator was a standard bell-jar type made by Perkin-Elmer with a Sloan PAK 8 electron gun used to bombard the target. The evaporation chamber contained a Sloan quartz crystal microbalance (frequency offset) thickness monitor.

Ion Implantation. This system implants energetic, charged particles (ions) into the sample. In this research effort, the purpose was to provide self-aligned doping in the source and drain regions. A block diagram of an ion implantation machine is shown in Figure 14. The implanter works by: using a mass separating analyzer to eliminate unwanted ions, accelerating the selected ions to high energies via an electric field, and then allowing the high energy ion beam of a controlled dose to impinge on the target. The ion implanter type was a Varian/Extrion Series 400-10A with a gas ion source. With this system, any element of atomic mass 1 to 200 can (in principle) be implanted with energies between 50 to 400 KeV. Below this energy, this implanter is not capable of producing a stable ion beam. However, it is

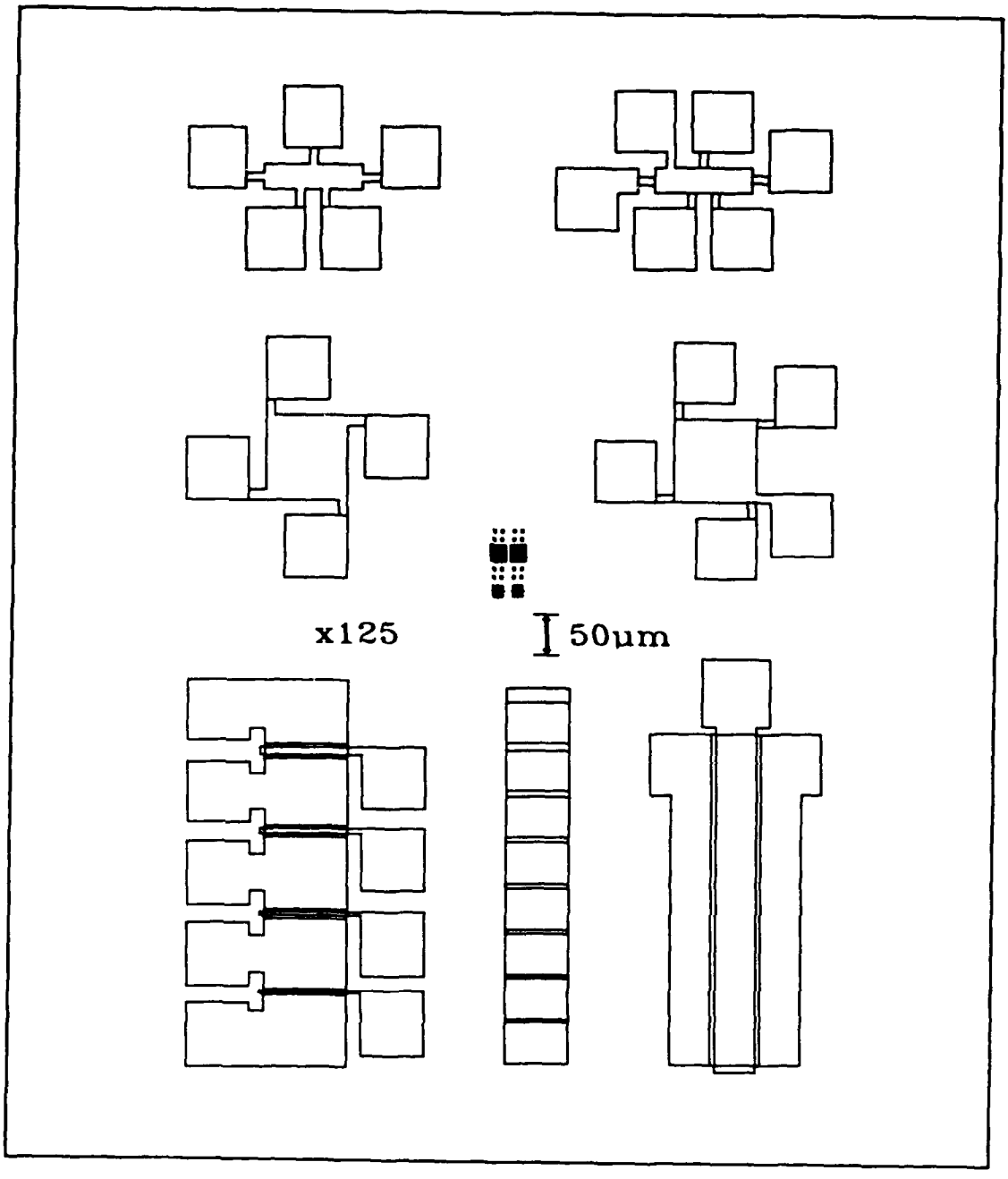


Figure 13. Overall Mask View of Finished Devices. Figure is 125 Times Actual Size

capable of producing doubly ionized atoms to almost double the implant range. Two implant chambers were available. The first is a research chamber which can hold four samples, each with a maximum diameter of 2.25 inches. The samples are mounted on a stage that can be cooled to 77 °K or heated to 600 °C. The samples can be tilted at any angle from 0 to 15 degrees off the normal to the ion beam [19;20]. This tilting is typically done to avoid ion channelling in either the <100> or <110> directions.

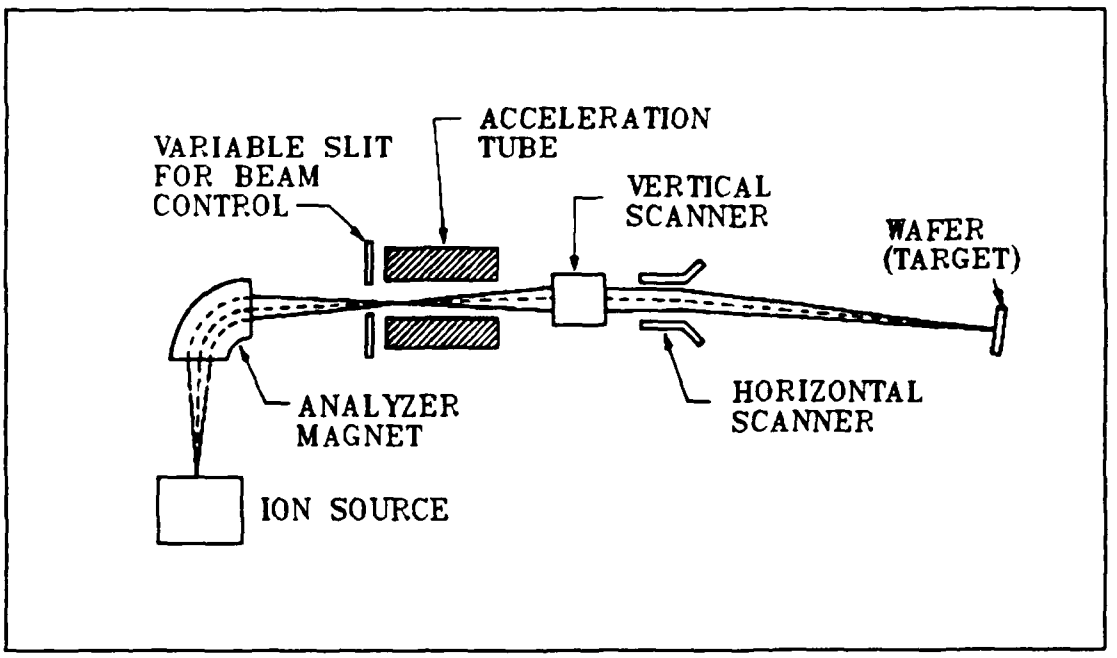


Figure 14. Schematic of a Typical Ion Implantation System [59:405]

Annealing. A Rapid Transit Anneal (RTA) system was used to thermally anneal the damage from implantation and to activate the implanted silicon dopant. The system used was

a Heatpulse 210T, which handles four inch diameter wafers and uses tungsten lamps. The RTA can heat a wafer from room temperature to over 1000 °C in a matter of 15 to 30 seconds, depending on the intensity setting. This unit had a silicon baseplate wafer with an embedded thermocouple and heating lamps on top and bottom. The keyboard controller is separate from the oven. The controller receives input from the thermocouple and responds by changing the intensity of the tungsten lamps according to a preset program. The instrument has an automatic mode which sets the lamp at 48% of the maximum intensity, ramps up to a preset temperature, holds that temperature for a preset time, and turns off the lamp. An atmosphere of forming gas, which contains 5% hydrogen, is maintained during the anneal process. This helps to keep the samples free from oxidizing in an environment of impurities [20;22].

Parameter Analyzer. The Hewlett-Packard model 4145 (A or B) Semiconductor Parameter Analyzer was used to determine the DC characteristics of the SISFET. This instrument has up to four channels, three of which were used to connect to source, drain, and gate of the SISFET via a probe station. The analyzer can be quickly switched from measuring I-V curves to transconductance or threshold voltage without changing any wires. Furthermore, the desired settings and sweep ranges for V_{DS}, V_G, and I_{DS} can be stored and recalled. Transconductance can be measured easily because the analyzer can calculate and

plot functions of variables as well. The analyzer is essentially a computerized curve tracer.

Impurity Profile. Two techniques were used to determine doping profiles after implantation. A capacitance-voltage (C-V) analysis can determine the majority carrier profile (which is the impurity profile assuming full ionization and 100% activation). This requires measuring the reverse bias capacitance of the p-n junction as a function of the applied voltage [59:391]. This was done using the capacitance-voltage analyzer at AFWAL. A more accurate and more sensitive technique, which can measure the total impurity profile, is called Secondary Ion Mass Spectroscopy (SIMS). In this technique, an ion beam sputters material from the surface of a sample in ultra-high vacuum, and the secondary ion component (from the sample) is detected and mass-analyzed. Ion counts for a particular element can then be directly equated to doping concentrations [59]. SIMS measurements were done both at AFWAL and at CSL in order to characterize the implantation of ^{+28}Si into GaAs.

Physical Profile. In addition to determining doping profile, the physical or dimensional profiles of the sample were determined throughout the fabrication. This was done using a TENCOR Alpha Step 200 profilometer at CSL. This instrument can respond to step differences on the order of 10's of Angstroms and, with reasonable accuracy, can determine step differences of 100's of Angstroms. The instrument has

a stylus which makes three passes over the sample. Then the slope of the profile is averaged and is subtracted internally from the stylus reading before the result is displayed.

Four-Point Probe. A simple way to measure the sheet resistance of a sample is with a four-point probe. The four-point probe used in this study was located at AFWAL, and it was used to measure sheet resistance after the annealing of implantation control samples. It is a Model 880 made by 4 Dimensions, Inc., for use on GaAs. The probes are equally spaced. A constant current is passed through the outer two probes, and the voltage is measured between the two inner probes. A value of sheet resistance is displayed. Sheet resistance is related to the junction depth, the carrier mobility, and the impurity distribution. The average resistivity of the sample is the sheet resistance times the junction depth [59:391].

SEM. The Scanning Electron Microscope (SEM) located at the AFIT Devices Laboratory was used in this study. It is an International Scientific Instruments (ISI) model SB-6. The instrument provides a high resolution and a high depth of field, which were necessary to examine the surface of our samples. The basic components of a SEM are the lens system, electron gun, electron collector, visual and recording CRT's, and the associated electronics. For this study, the use of the SEM was to verify the dimensions and surface properties of the samples after fabrication [18;21].

TEM. The JEOL 2000FX Transmission Electron Microscope (TEM) located at AFWAL (Materials Lab) was also used in this study. The 2000FX has a 200 kV maximum accelerating potential. From the de Broglie relation, an electron accelerated with this energy has a relativistically corrected wavelength of 0.0251 Å. This small wavelength, as compared to 0.0370 Å for a 100 kV potential, translates to either increased resolution or to the ability to examine thicker samples with the same resolution. A TEM has a series of magnetic lenses to focus an electron beam that is accelerated through the sample (in a vacuum) by a high potential. The TEM was used to verify the quality of the MBE layers grown for this study. Additionally it provided information about the implantation and annealing processes. The features of a typical TEM are shown in Figure 15 [13:1;61].

An electrically heated tungsten filament, at a selected negative potential 20-200 kV, is mounted on a ceramic insulator behind a Wehnelt cap with a central hole. The electrons emitted by the filament accelerate to ground and are focussed, via a double condenser lens system with field-limiting apertures, onto the sample [13:1]. Since electrons have a wave nature, a diffraction pattern results and is obtained via a multiple lens magnification sub-system. Image contrast is enhanced by the objective aperture, and the selected area aperture selects the diffraction area. The image is focused with the objective lens onto the viewing

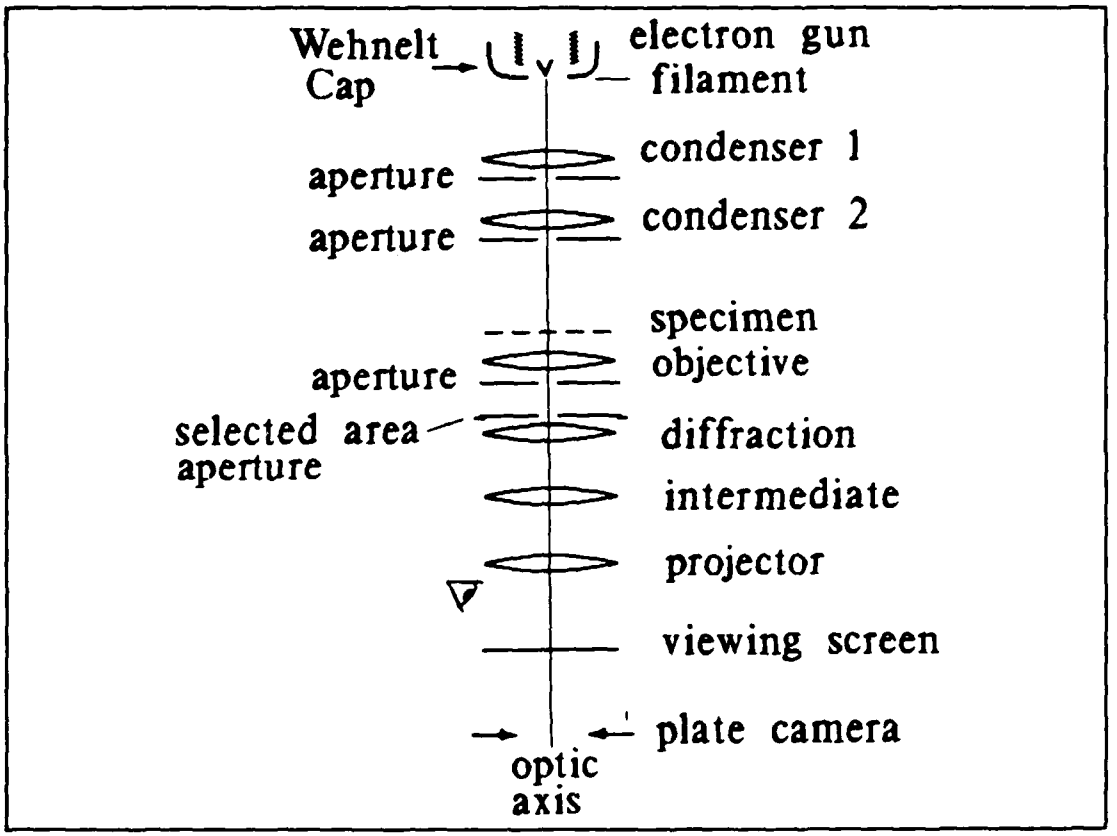


Figure 15. A Schematic Diagram Showing the Important Components of the Transmission Electron Microscope [13:2]

screen. Excitation of the intermediate and/or diffraction lens controls the magnification [13:1]. The depth of field with the TEM is such that the top and bottom of the sample are simultaneously in focus. This feature allows the film camera to be situated 50 cm or more below the viewing screen [13:1].

SISFET Fabrication

This process is logically divided into five sequences: MBE growth, gate deposition, ion implantation, annealing, and

source/drain deposition. The following sub-sections deal with these fabrication steps. If not explicitly stated otherwise, all these steps were performed at room temperature and all solutions were at room temperature.

MBE Growth. The semiconductor layers were grown by MBE at CSL. The graduate students there cleaved undoped, semi-insulating, (100) oriented GaAs substrates into nearly square pieces approximately 2.5 cm on a side. The samples were etched 30 seconds in an $H_2SO_4:H_2O_2:H_2O$ (10:1:1) solution and then placed in HCl for one minute. The samples were immersed in these solutions to clean and remove any surface oxides. Next, a single square sample was rinsed in De-Ionized Water (DIW), dried with N_2 gas, and mounted on a molybdenum block with indium solder which was applied to the back of the substrate. It was then loaded into the MBE chamber. Different growth runs were accomplished in accordance with the various test parameters which are presented in Chapter IV.

Although not part of the actual MBE growth process, some simple preparation steps followed the MBE growth. Individual samples were cleaved from the prepared layers using a diamond tipped scribe. These samples were labeled 1, 2, etc. Before processing, it was necessary to remove the indium solder from the backside of the samples. A solution of 1 gm $HgCl_2$ (mercuric chloride) and 10 ml of $HCON(CH_3)_2$ (dimethyl formamide) was used. After the samples were placed in a beaker containing this solution, the combination was

immediately placed in an ultrasonic bath. After 20 seconds, the samples were removed from the solution, rinsed in DIW, and blown dry in N_2. Alconox detergent was used to remove any residual Hg. A subsequent degreasing in acetone, methanol, and DIW insured that the Alconox was removed. The samples were not lapped. Moisture was baked out at 110 °C for 5 minutes.

Gate Deposition. Positive photoresist (PR) type 4110 was spun on a sample at 5000 rpm for 30 seconds. The sample was pre-baked at 70 °C for 20 minutes, exposed to the gate mask for 13 seconds, soaked in chlorobenzene for 15 minutes, and developed in an AZ400K developer to DIW (3.5:1) solution for 3.5 minutes. Chlorobenzene was used to harden the surface of the PR so that the developing process produces a slight lip over the undeveloped region. This feature allows less sidewall buildup during the metallic contact evaporation process and provides for a clean liftoff with thick depositions. The gate mask is shown in Figure 16.

The sample was cleaned in a 10% NH_4OH (ammonium hydroxide) solution, and placed in the evaporation chamber. The process involved mounting the samples, placing the metal pellets to be deposited in the appropriate crucibles, checking the seal, and then evacuating the chamber to 10^{-6} torr or less. The chamber was pumped down to approximately $3x10^{-7}$ torr, and approximately 2000 Å of molybdenum was evaporated on the sample according to the thickness monitor. Thickness

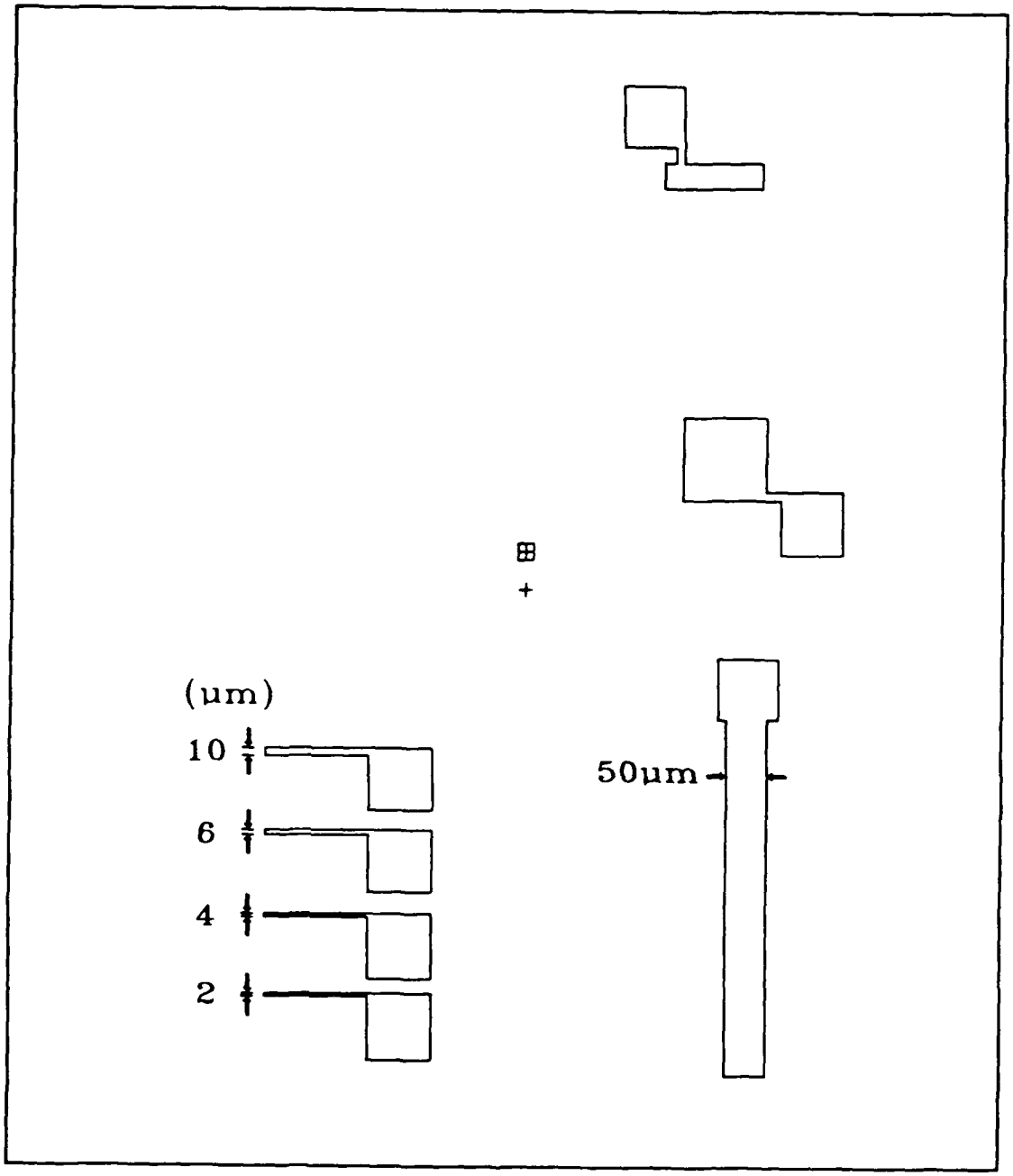


Figure 16. Molybdenum Gate Deposition Mask Pattern

measurements taken with a profilometer confirmed these numbers. The chamber was cooled for 15 minutes, and then the samples were removed. Liftoff of the unwanted metal was accomplished with a 15 second ultrasonic bath in acetone. Molybdenum was used because it is a refractory metal, very dense, and melts at 2610 °C. Thus, it can block the implant and withstand the high temperatures associated with annealing. The result of the gate deposition process is illustrated by the device cross section in Figure 17.

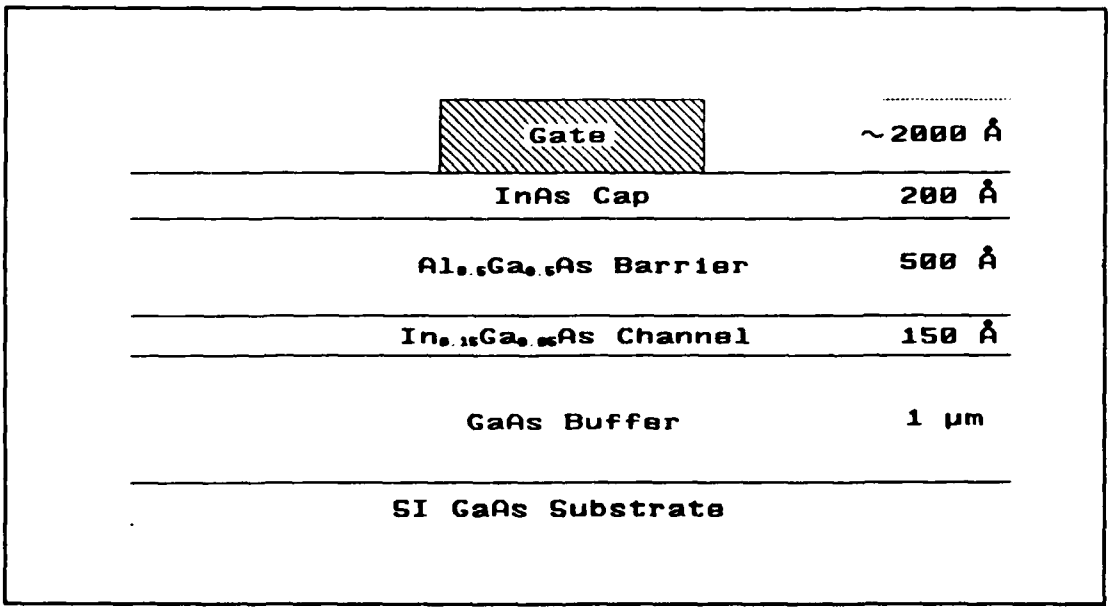


Figure 17. Cross Section After Gate Deposition Process

The samples were degreased in acetone, methanol, and DIW. Then they were etched for 15 seconds in a 1:1:38 solution of H_3PO_4:H_2O_2:H_2O. This is a standard indium and aluminum etch which removes InAs at approximately 20 Å per second and AlGaAs at approximately 14 Å per second [36;47;51]. This procedure

produces a self aligned etch of the capping layer and etches into the AlGaAs barrier layer approximately 75 to 100 Å. The device cross section in Figure 18 illustrates the result of the self-aligned etch process.

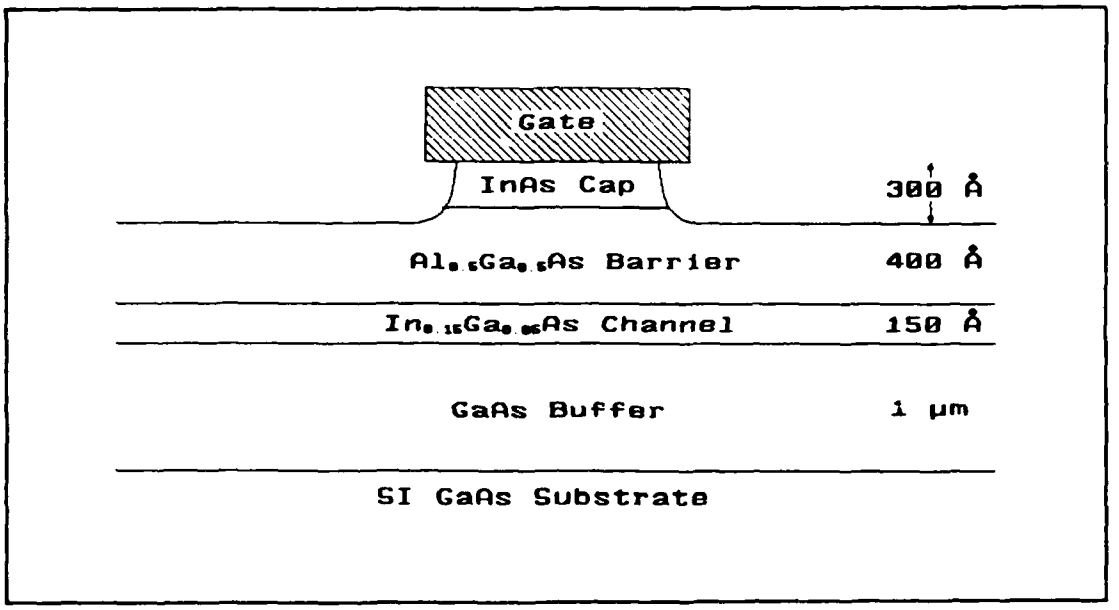


Figure 18. Cross Section after Self-Aligned Capping Layer Etch

Ion Implantation. The ion implantation steps proceeded as follows. Samples were degreased in 30 second rinses of acetone, methanol, and isopropyl alcohol and then blown dry with N_2. It was assumed that the isopropyl alcohol did not leave a residue. The sample was placed in the implanter such that the tilt angle was along the width of the transistor gates and was fastened via movable metal pieces and screws. The operator at AFWAL pumped down the chamber and implanted the various samples at energies ranging from 60 KeV to 100 KeV

and at an ion flux ranging from 1 x 10^{13} cm^{-2} to 5 x 10^{13} cm^{-2}. The samples were tilted off normal at an angle of 7 degrees so that channeling in the <100> directions would be minimized. The samples were implanted with ^{+28}Si ions. Figure 19 shows a cross section of the implanted regions of the device.

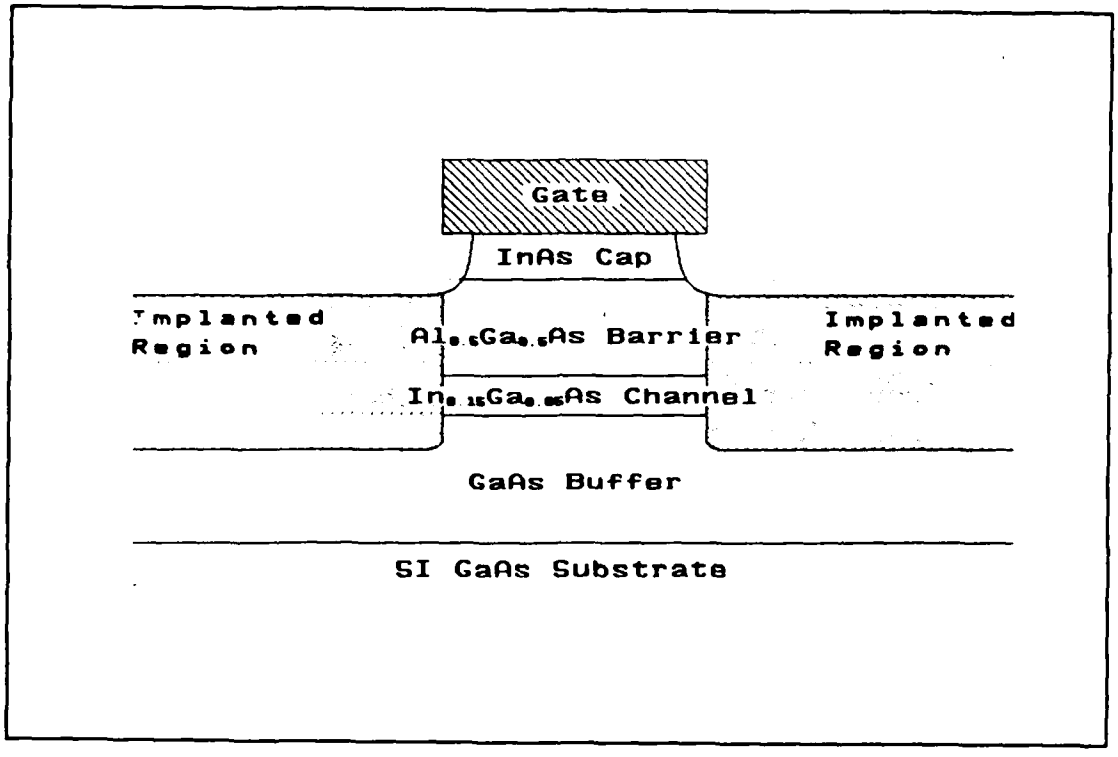


Figure 19. Cross Section of Implanted Region of SISFET Device

Annealing. The annealing steps proceeded as follows. The samples and a two inch silicon wafer were degreased in 30 second rinses of acetone, methanol, and isopropyl alcohol and then blown dry with N_2. A two inch undoped GaAs wafer was etched for 30 seconds in a 10:1:1 solution of H_2SO_4:H_2O_2:H_2O solution to obtain a clean surface, and baked at 100 °C for

5 minutes in an N_2 atmosphere. The arrangement of these wafers and the samples in the RTA is represented in Figure 20.

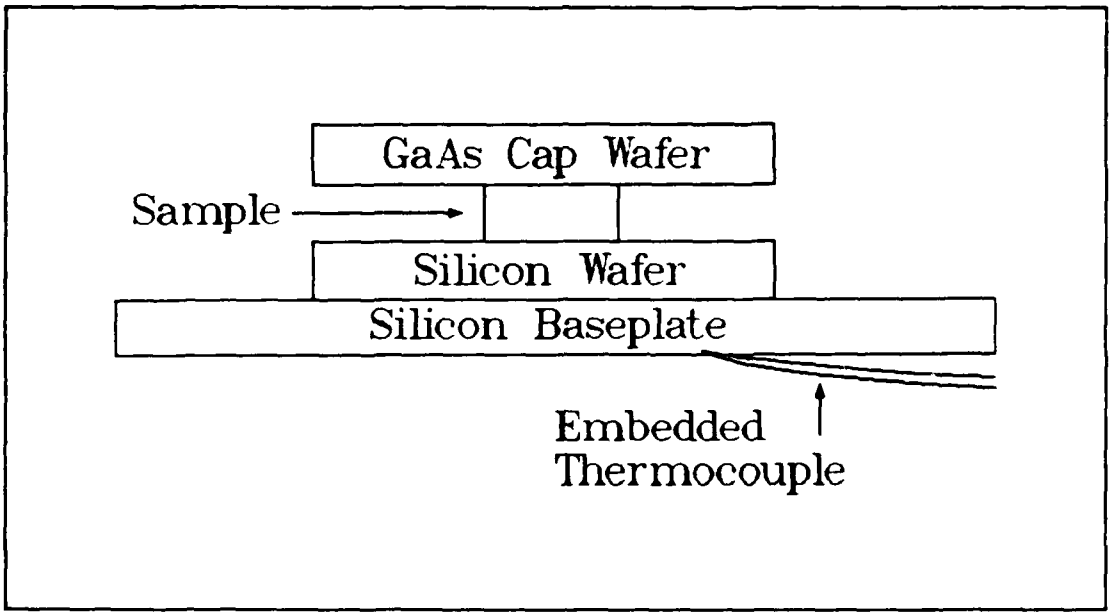


Figure 20. Arrangement of Wafers and Sample During Rapid Transit Annealing (RTA)

The silicon wafer was placed face up on top of the silicon baseplate in the RTA chamber. The sample was placed on the silicon wafer face up, and then a GaAs cap wafer was placed on the sample face down. This arrangement allows for a clean GaAs surface to contact the device side of the sample in order to maintain a local over-pressure of As during the anneal process. The chamber was then sealed. The RTA unit was activated and programmed for a ramped temperature cycle. The anneal was done in an atmosphere of forming gas. The automatic thermocouple mode was used to provide more consistent and repeatable control of the temperature. The

alternative involves adjusting the intensity of the lamps manually. Throughout this effort, the annealing temperatures ranged from 600 °C to 850 °C, and annealing times ranged from 2 seconds to 15 seconds. These test parameters and a description of thermocouple position with respect to the sample are summarized in Chapter IV.

Source and Drain Deposition. The source and drain deposition proceeded as follows. The samples were thinned uniformly to an approximate thickness of 400 μm using a metal lapping block and paraffin wax adhesive. This step facilitated accurate photolithographic mask alignment of the mesa mask and the source and drain mask. Positive PR (AZ1350J) was spun on the sample at 5000 rpm for 30 seconds using the spinner. The sample was pre-baked at 90 °C for 20 minutes, exposed to the mesa mask for 7.5 seconds, and developed in a 1:5 solution of AZ351 developer to DIW for 60 seconds. The mesa mask is shown in Figure 21. The sample was rinsed in DIW and blown dry in N_2. A mesa isolation etch was done for 100 seconds in a 1:1:38 solution of H_3PO_4:H_2O_2:H_2O. This etch goes well into the GaAs buffer and probably into the semi-insulating substrate which is necessary to have good device isolation. The PR was stripped by rinsing in acetone, and more of the same PR was spun on. The sample was exposed to the source/drain mask, shown in Figure 22, for 7.5 seconds and developed in the same developer for 60 seconds.

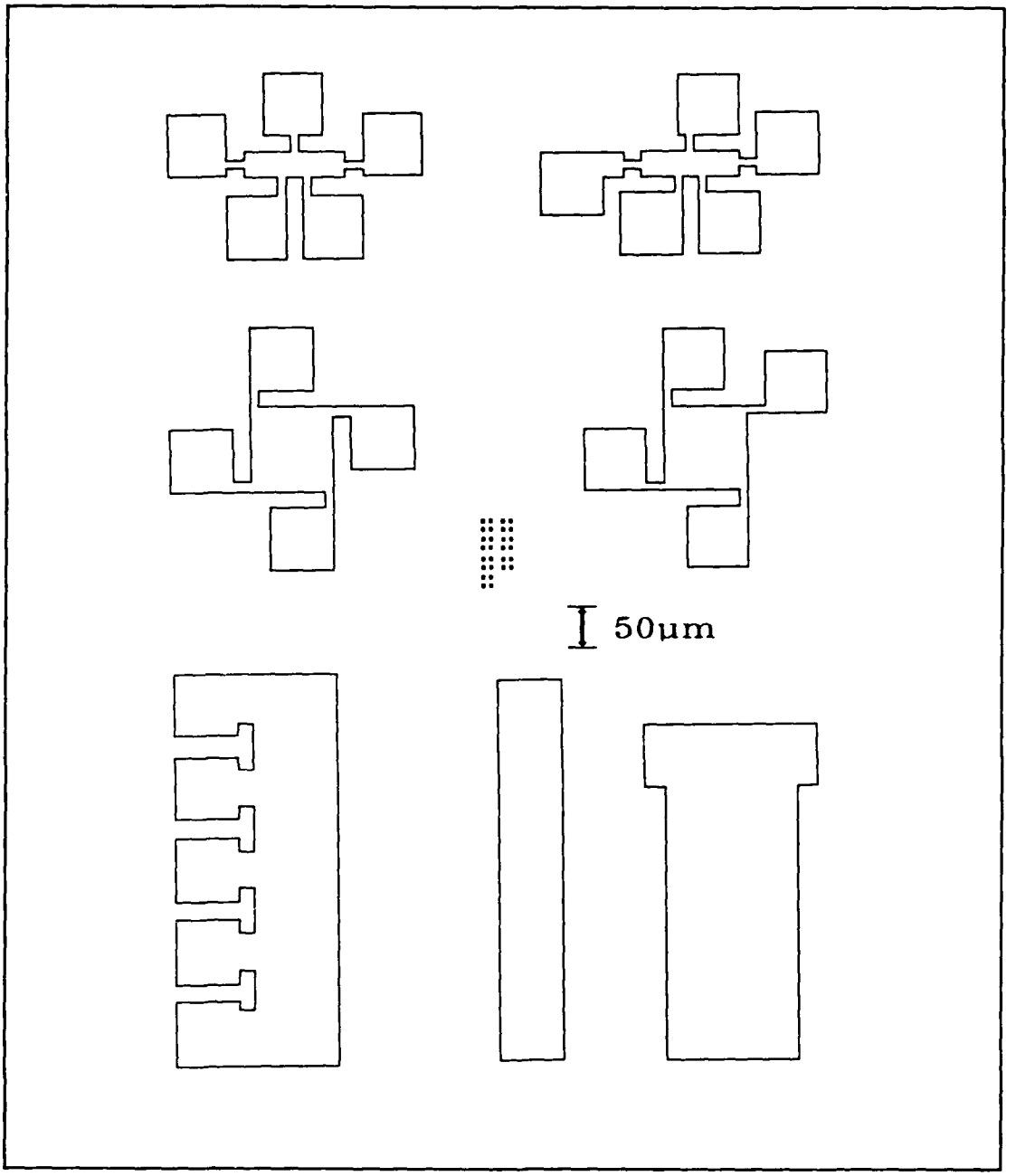


Figure 21. Mesa Device Isolation Mask Pattern

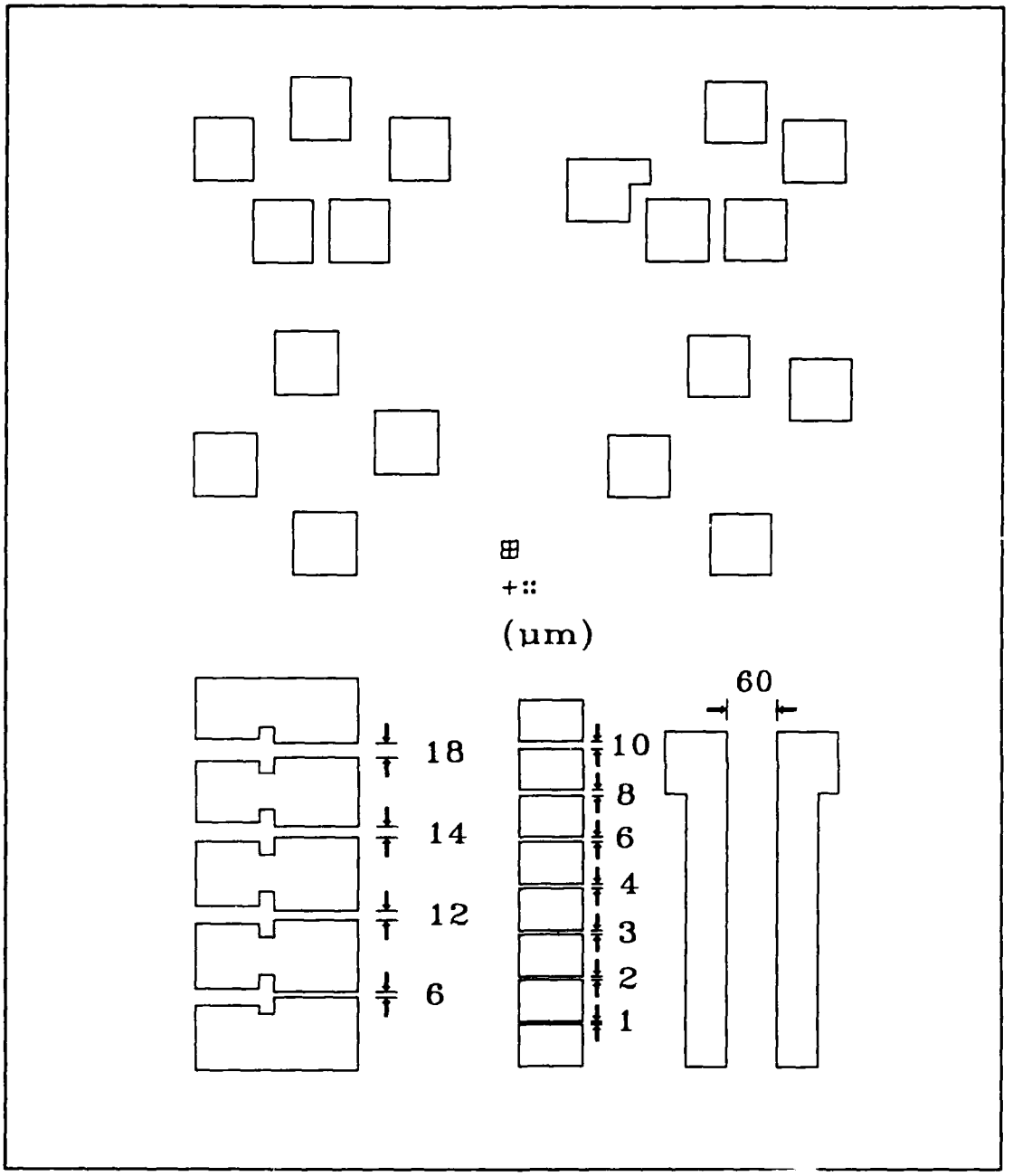


Figure 22. Source and Drain Contact Mask Pattern

Prior to the actual deposition, the sample was cleaned for 15 seconds in a 10% NH_4OH solution. Various samples were loaded into the evaporation chamber. The chamber was evacuated to approximately 10^{-6} torr and 400 Å of AuGe, 100 Å of Ni, and 500 Å of Au were deposited on the sample in that order. The chamber was cooled for 15 minutes, and then the samples were removed. The sample was placed in a beaker of acetone and rinsed for 15 seconds in an ultrasonic bath. This removed the unwanted metal in the regions where the photoresist had been exposed and developed. The cross section of the device after the source and drain deposition procedure is shown in Figure 23.

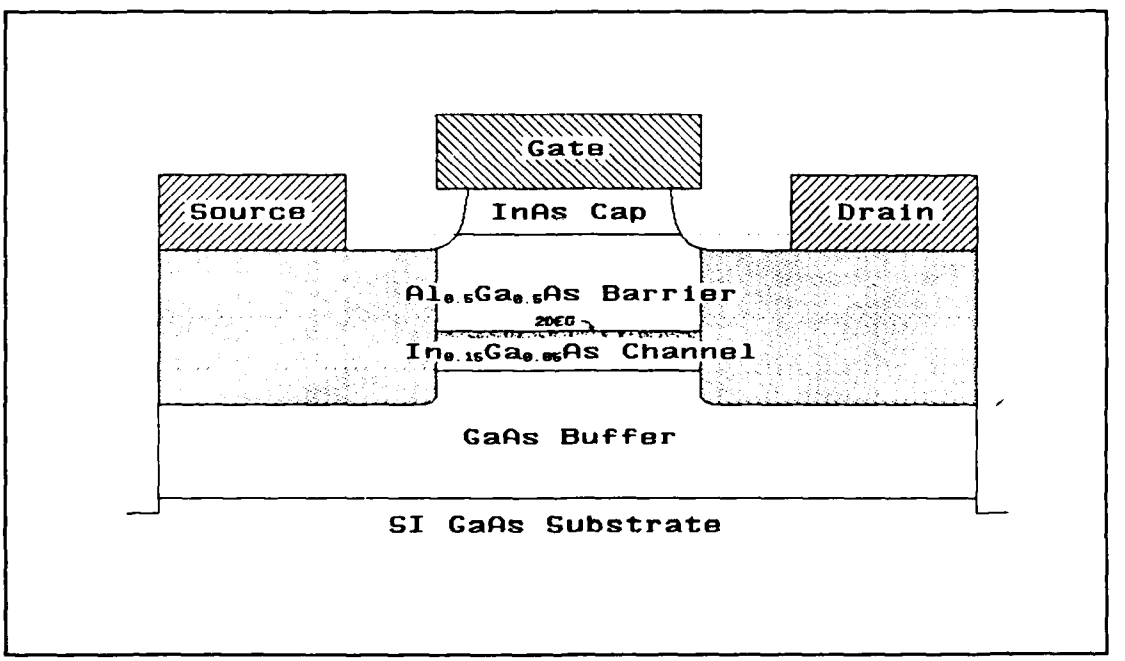


Figure 23. Device Cross-Section after Deposition and Liftoff

Finally, the source and drain contacts were alloyed to produce ohmic contacts. The idea is for the Ge in the metal eutectic to diffuse into the doped (implanted) region, making the contacts highly n-type. The alloying oven was heated to 500 °C, and the samples were placed inside the glass tube. The oven was purged with nitrogen for 3 minutes before pushing the sample into the heat for 50 seconds. The samples were then pulled back to the original position inside the tube. As the samples cooled, the oven was purged with nitrogen for 3 minutes before the samples were removed. This was the last step in the fabrication process. An overall mask view of the devices was shown previously in Figure 13.

IV. Characterization and Analysis of the Self-Aligned, Strained-Channel SISFET Fabrication

Purpose

This chapter presents a description of any test setups along with test results. Because the devices did not work as expected, no attempt is made to present, in detail, the results of any DC measurements. Therefore, rather than any device characteristics, the thrust of the test results is to confirm either the validity or lack thereof of the individual steps in the fabrication process.

Overview

Given the purpose stated above, the presentation of information is according to the steps in the fabrication process as described in Chapter III. The corresponding sections are: MBE growth, TEM investigation, gate deposition, ion implantation, annealing, and source and drain deposition. Each section includes a description of the steps that were taken to check the validity of that particular step. A final section deals with the finished devices. It presents some SEM pictures as well as the DC characteristics that were measurable.

MBE Growth

Undoped semi-insulating (100) oriented GaAs substrates were prepared in accordance with the description of MBE growth in Chapter III. This effort consisted of two test growth

runs, and the Coordinated Sciences Lab (CSL) designators for these MBE layers were 3409 and 3903. The layers were grown in accordance with the experimental parameters listed in Table 2. It shows the effusion cell temperatures, thicknesses, mole fractions, and doping level for each layer, as appropriate. Also shown is the As effusion cell temperature which is set to maintain an over-pressure of As in order to achieve high quality growth. The arrows represent a ramping (up or down) of this temperature in order to maintain a constant over-pressure.

In general, for purposes of fabrication, it was assumed that the material from the MBE growth runs satisfied the specifications in Table 2. In the MBE process, a given set of growth parameters can produce consistent and proven results. Additionally, the CSL personnel have historically produced good MBE material. Thus it was also assumed, at the start and throughout most of this effort, that the MBE process resulted in good quality crystal layers. However, given the lack of success in making working transistors, these two assumptions were potentially bad ones.

Therefore, this study included a TEM analysis which is presented in the next section. These TEM results show the invalidity of the above assumptions at least with respect to layer 3903. Other factors contributed to the conclusion that the material was not what was expected. This will be discussed more, but several qualitative observations are worth

Table 2. MBE Growth Run Parameters for Layers 3409 and 3903. Arrows Represent Ramping Temperatures Over Time

MBE 3409 Layers				
	1	2	3	4
Effusion Cell Type		Effusion Cell Temperature (°C)		
Ga	925	863	863	-
Al	-	-	1071	-
Si	-	-	-	1121
In	-	680	-	740
Thickness	1 μm	150 Å	500 Å	200 Å
Mole Fraction	-	0.15	0.5	-
Doping Level	-	-	-	$5x10^{18}$ cm^{-3}
As Cell (°C)	580	↓550	↑610	↓550

MBE 3903 Layers				
	1	2	3	4
Effusion Cell Type		Effusion Cell Temperature (°C)		
Ga	926	873	873	-
Al	-	-	1070	-
Si	-	-	-	1123
In	-	666	-	725
Thickness	1 μm	150 Å	530 Å	500 Å
Mole Fraction	-	0.15	0.5	-
Doping Level	-	-	-	$5x10^{18}$ cm^{-3}
As Cell (°C)	580	↓530	↑600	↓490

mentioning. First, the appearance of layer 3903 was hazy, while layer 3409 was mirror-like. Second, layer 3903 was one of the first layers grown after correcting a problem with the aluminum effusion cell. Third, after much of the fabrication had been attempted with 3903, other problems became apparent. One definite problem was that the thermocouple which detects the substrate temperature was out of calibration, perhaps by as much as 30 °C from the optimal temperature for good quality crystal growth. This became known after layer 3903 had already been grown and after three fabrication attempts. The other potential problem was that the depletion of the aluminum effusion cell was not properly corrected before layer 3903 was grown. Although CSL personnel believed they corrected the problem, it is questionable given the following TEM results.

TEM Investigation

This study involved three different attempts to characterize the quality of the MBE material through TEM. The first two attempts were inconclusive, and will not be presented here in detail. However, they are worth brief mention. After the transistors fabricated from 3409-1 did not work as expected, the sample was prepared and analyzed in the TEM. The resulting diffraction patterns showed polycrystalline structure everywhere. However, that finished sample had undergone ion implantation, and it was not clear exactly what region (i.e., implanted or active) was being observed in the TEM. It was concluded that if the damage from implantation

had not been annealed, the expected result could be the observed result.

This led to a more careful consideration of the annealing conditions. Still, there was no reason to assume that the 3409 MBE layers were faulty. Different parameters were changed throughout the next two fabrications. The result on 3409-4 was hopeful. The transistor characteristics looked good and the gate leakage was very low. The main problem remaining was that the contacts were not good ohmic contacts. However, at this point in the study, the 3409 sample was gone and a new layer needed to be grown.

This lead to the second TEM study. The new layer (3903) was grown, and in order to solve the contact resistance problem, an annealing study was undertaken. The result was reasonably good ohmic contacts. But no transistor characteristics were achieved with either 3903-1 or 3903-2. Consequently, the MBE layers became suspect, and a piece of 3903-2 (before ion implantation) was analyzed. The sample was prepared by mechanically dimpling the underside of the sample and then ion milling the underside so as to preserve the device structure.

The results were that material interfaces were observed. The bright field micrographs, the diffraction patterns, and the X-ray spectrum gave "indications" of a problem. For example, the semiconductor regions were indexed (as will be described later in this section) to a beam direction of

[$\bar{1}$ 0 0] for GaAs with one percent of error. This was the expected result for an electron beam normal to the top surface of the sample. However, there were extra bright spots (not rings) which were not indexable leading to the hypothesis that some other material(s) were contributing to the pattern.

The gate region diffraction patterns were rings which were accurately indexed to molybdenum. Thus, it was known that the gate metal was not contributing to this ambiguity. Additionally, the higher resolution bright field photomicrographs revealed grain structures. This method did not lead to a conclusive determination because of the inability to accurately determine exactly what semiconductor materials or interfaces were being observed. Logically, the third TEM investigation of the MBE layers involved examining the cross section of the material. To accomplish this objective, a piece of sample 3903 that had not undergone any processing was used.

Sample Preparation. This third sample was prepared by microtomy, which is the direct cutting of thin sections. The objective was to obtain a thin cross-section of the substrate and layers. This involved embedding the sample in a polymer holding block. The polymer hardens around the sample when placed in a vacuum oven. Next, the sample was microtomed using a Reichert-Jung ULTRACUT Microtome. The cutting is done as the sample in the holding block moves past a stationary diamond knife. The knife can be set in relation to the

cutting surface of the specimen, and the holding block can be rotated. This allows complete flexibility of the cutting angle.

The resulting TEM sections from layer 3903 were very close to 90° cross sections of the substrate and layers. The thicknesses were determined to be between 700 and 900 Å by observing the color of the refracted light in the microtome's microscope. When the sample is cut, the piece(s) float on a water reservoir located by the knife edge. They are then scooped onto a carbon film which is supported by a nickel grid. It is acknowledged that microtoming may not be the best way to analyze a semiconductor crystal. Microtoming can introduce dislocations, and it results in shavings of a cross-section as opposed to a complete cross section. However, the result of this method, in this case, was conclusive.

Bright Field Micrographs. Diffraction (or amplitude) contrast is the mechanism for producing Bright Field (BF) micrographs. The diffracted beam of the TEM is intercepted by the objective aperture and not allowed to contribute to the image. Instead, the transmitted beam forms the image. Diffraction contrast delineates object detail greater than 15 Å in crystalline materials, and can provide information about defects in the crystal [13:109]. BF images can reveal the presence of such things as dislocations, stacking faults, planar precipitates, and domain boundaries. For this study, diffraction contrast was used simply to observe the presence

of interfaces or layers in the material. Once these interfaces were detected, selected area diffraction patterns of the interface regions were obtained.

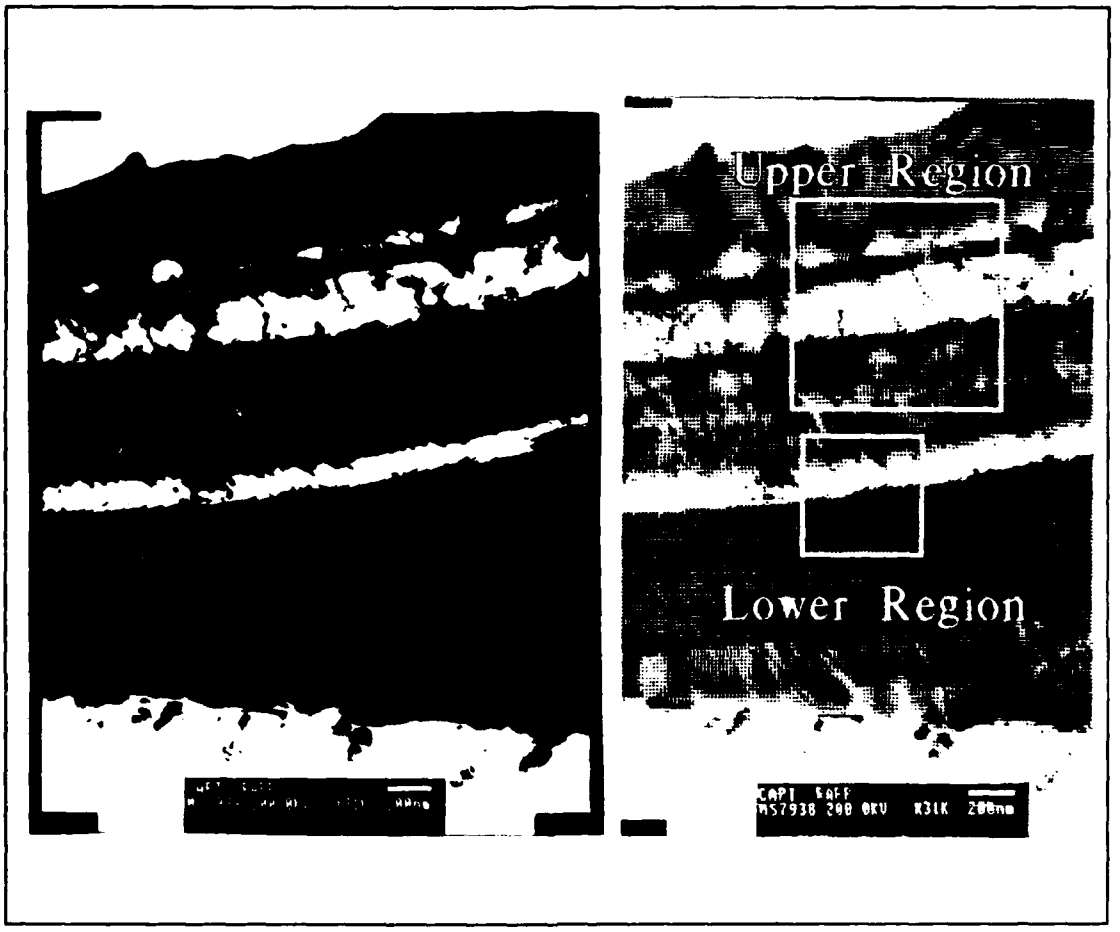


Figure 24. Bright Field TEM Micrograph Showing Cross-Section of MBE Layer 3903

A BF image of one of the cross sections is shown in Figure 24. The results presented here are a small subset of the effort expended to characterize the MBE layers. These particular images were selected because they give the most

accurate representation of the problem with the material. They are consistent with the total number of specimens that were examined. In this BF image, there are clearly a number of material interfaces visible. The interfaces are incoherent, and thus the most useful information is obtainable using selected area diffraction. The dimensions of these interfaces cannot be correlated to the "expected" dimensions of the layers. However, no other interfaces (substantially different from this) were found in the four grids that were examined. Each grid contained a number of microtomed cross sections. Figure 25 and Figure 26 contain two BF patterns magnifying the interfaces near the lower and upper lighter regions (respectively).

One can observe that the dimensions of these regions are on the order of 1000 Å or so. The significance of these regions will become apparent with the analysis of the corresponding selected area diffraction patterns. Also, a close inspection of Figure 24 reveals a number of generally straight and continuous lines running parallel to the interfaces. These are knife marks, and they are an artifact from the microtoming process.

Diffraction Patterns. Phase contrast is the mechanism for producing selected area Diffraction Pattern (DP) micrographs. Here, the diffracted and transmitted beams are combined to form the image. Constructive and destructive interference produced intensity differences in the image. The

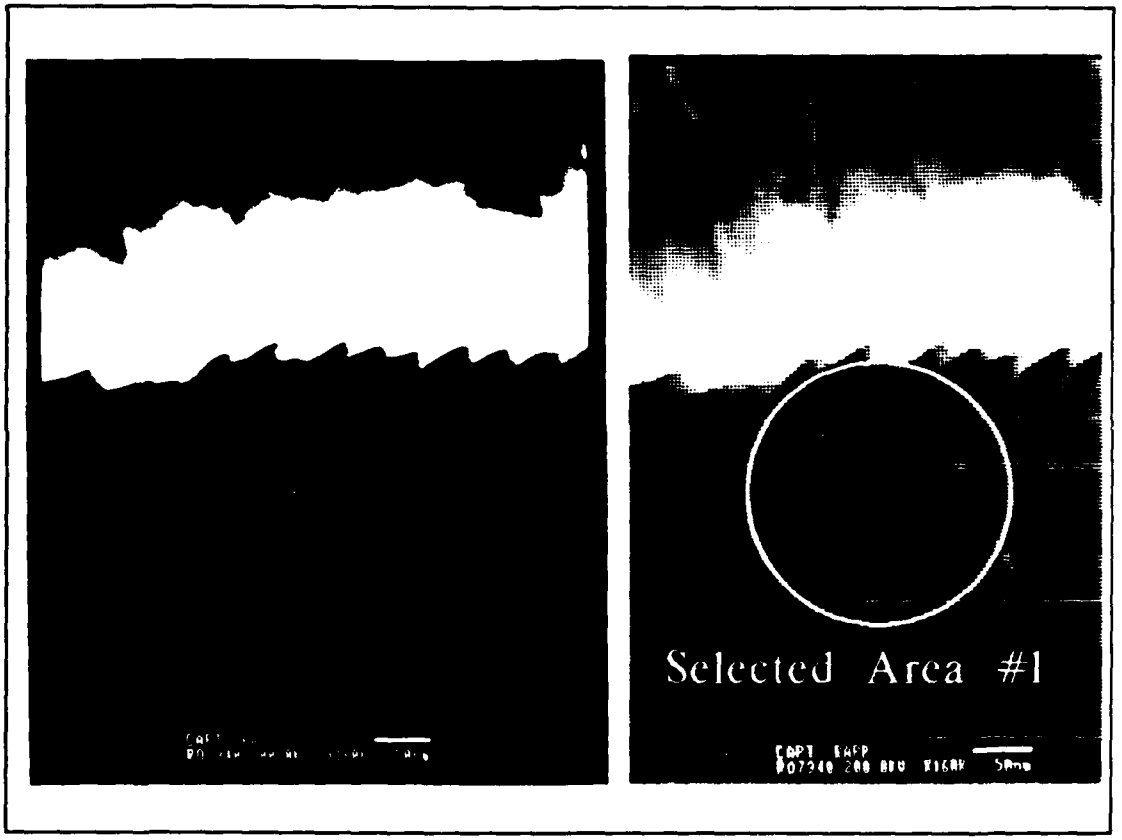


Figure 25. Magnified Bright Field TEM Micrograph of Lower Interfaces in Cross Section of MBE Layer 3903

image is actually the Fourier transform of the diffraction pattern. Thus, it provides a view of a crystal (or specimen) in reciprocal space. The condition for diffraction or constructive interference is Bragg's law [8:82]. If there are crystal planes oriented at a critical angle with respect to the incoming electron beam, there is a strong diffracted beam on the exit side of the crystal. Further, since the wavelength of a high energy electron is small, the Bragg angles are small. This means that strong diffraction only

occurs for planes that lie within a few degrees of the electron beam. Also, for a given type of crystal structure, the structure factor describes the contribution of the entire unit cell to the diffracted intensity. It is the sum of the scattering factors and phase differences for each atom in the unit cell. Structure factor effects result in certain types of reflections being absent from the diffraction pattern [13:31-183;28:42;62:13-138].

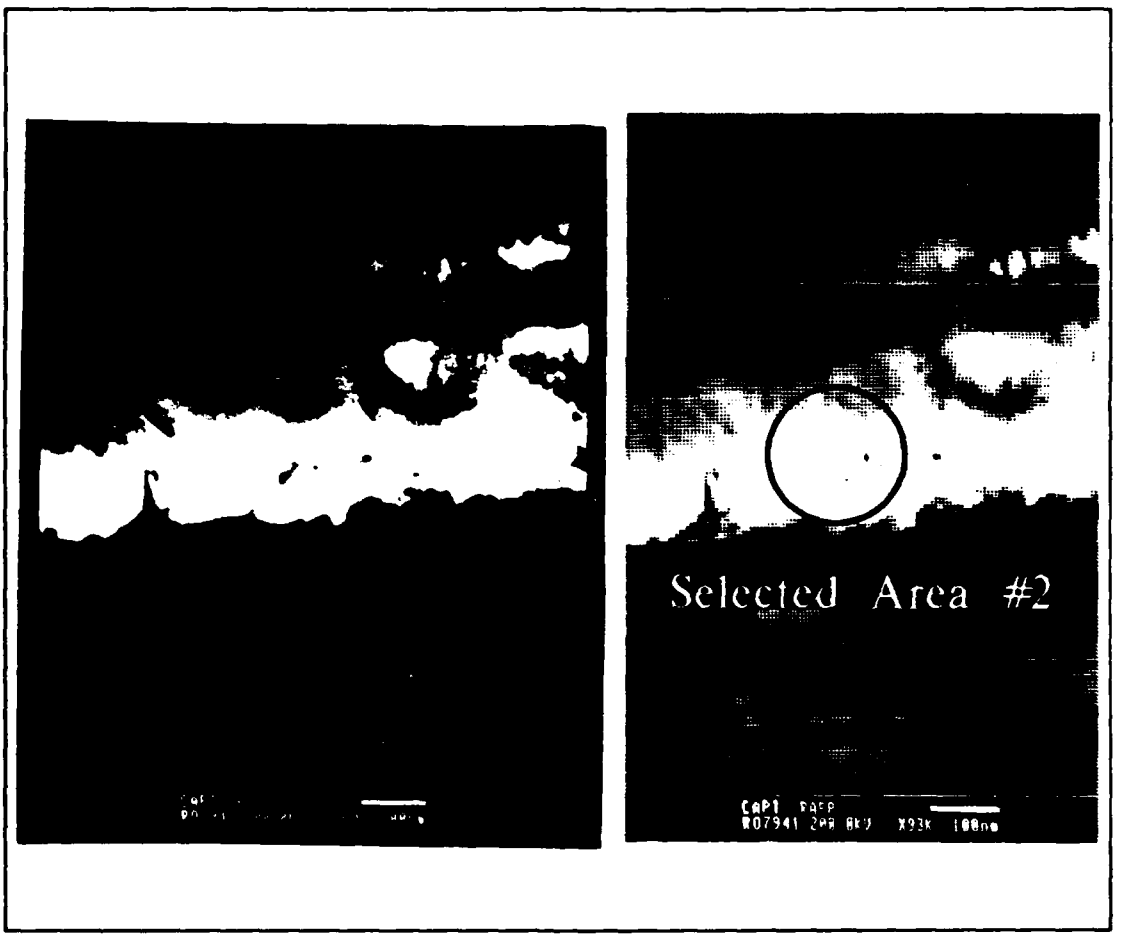


Figure 26. Magnified Bright Field TEM Micrograph of Upper Interfaces in Cross Section of MBE Layer 3903

The first step in analyzing any diffraction pattern involves a calibration. A camera constant must be determined such that the distance from diffracted spots to the transmitted spot may be translated to interatomic spacings between planes. For this study, the camera constant was calculated using an aluminum diffraction standard. The standard is polycrystalline so all the spots (reflections from the different planes) result in a ring pattern. However, this standard pattern is easily indexed using a modified form of Bragg's law. This is written as:

$$r \cdot d_i = \lambda \cdot l \qquad (\text{Å} \cdot \text{cm})$$

where: r = radius of spot or ring (cm)

d_i = interatomic spacing between lattice planes (Å)

λ = wavelength of the electron (Å)

l = TEM focal length (cm)

$\lambda \cdot l$ = camera constant (Å·cm)

The diffraction pattern of the aluminum standard is shown in Figure 27. The radius of each ring was determined by measuring the diameter and dividing by two. Cross correlation to a list of known d_i spacings for the lattice constant of aluminum yields a value for the camera constant. Five rings were measured, and the average camera constant was 2.03 Å·cm. This correlates with the product of the relativistically corrected wavelength of 0.0251 Å at 200 KV and the estimated

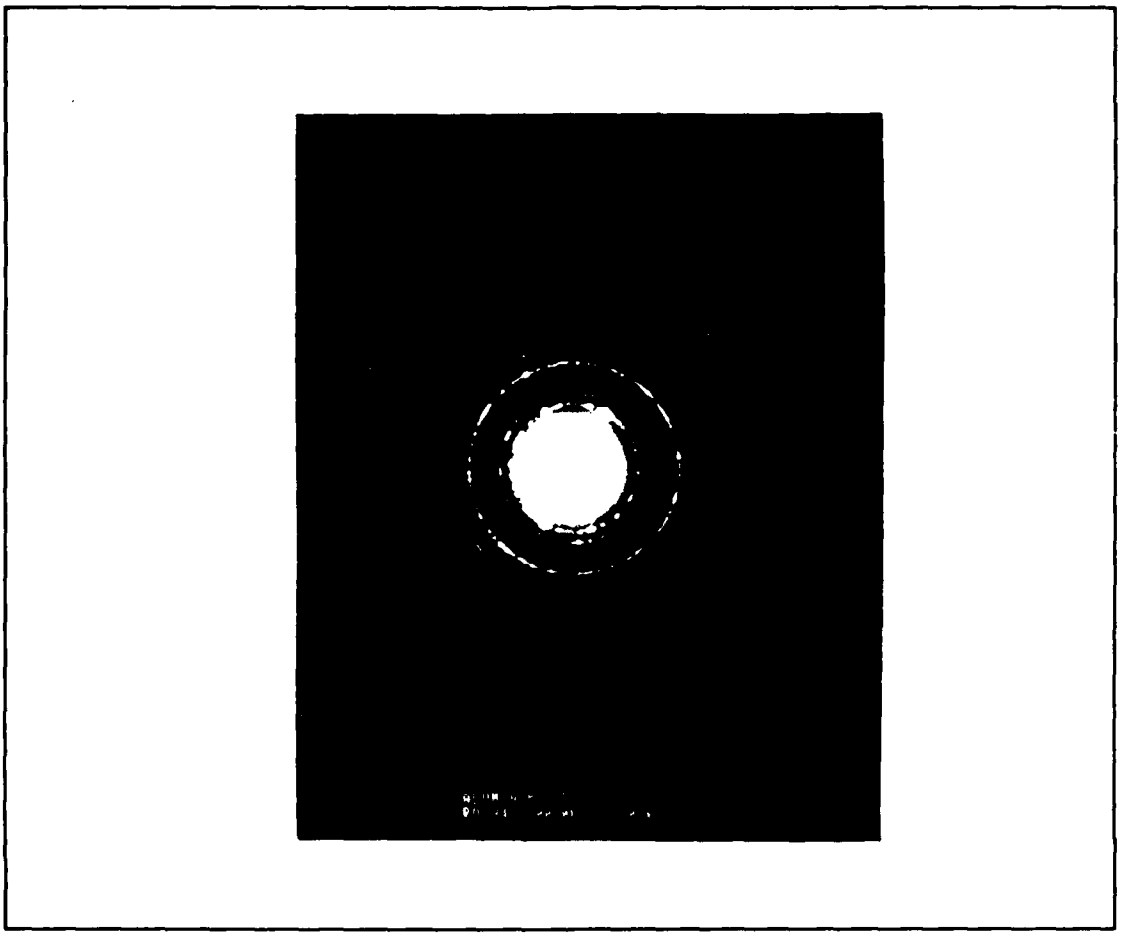


Figure 27. TEM Diffraction Pattern of Aluminum Standard Used for Calculation of Camera Constant

focal length of 77.0 cm on the picture. This product is 1.93 Å·cm which implies that the effective camera length is actually closer to 80.9 cm. The error associated with the measured d_i spacings using $\lambda \cdot l$ = 2.03 Å·cm and a_o = 4.05 Å is summarized in Table 3.

For a spot pattern, the spots represent an (hkl) plane in reciprocal space. Thus each spot may be mapped to a

Table 3. Summary of Errors Associated with Aluminum Standard Calibration Diffraction Pattern Using $\lambda \cdot l = 2.03$ Å·cm

	d_i spacings (Å)		
Plane	Measured	Calculated	Error
(1 1 1)	2.325	2.338	-0.56%
(0 0 2)	2.046	2.025	+1.04%
(0 2 2)	1.421	1.432	-0.77%
(1 1 3)	1.218	1.221	-0.26%
(2 2 2)	1.173	1.169	+0.34%

particular plane. If the material has a regular crystal structure, the spots will be in a regular or periodic array. Thus, one spot may be arbitrarily assigned an (hkl) index based on its radius and the other spots will correspond to specific (hkl) such that the indices add vectorially. Additionally, the angles between lines drawn from the center spot to individual (hkl) spots are the angles between planes. These angles may be calculated if the indices and crystal type are known.

Thus, if the following three tests are applied, the material and its orientation with respect to the electron beam can be accurately determined [33:4-17]. First, the d_i spacings must closely match the spacings for a particular material. From this, general (hkl) indices may be assigned. Second, specific (hkl) indices must be assigned to the spots

such that they add vectorially. Third the angles between specific (hkl) planes must correlate with the angles between lines drawn through those spots.

Two diffraction patterns which correspond to the selected areas (#1 and #2) in the BF micrographs of Figure 25 and Figure 26 were analyzed to within a one percent error. The first pattern was accomplished for the lower darker region (area #1) of the interface that was shown in Figure 25. The sequence numbers of these photographs are different because the sample had to be tilted a few degrees of axis in order to obtain an analyzable pattern, and this took several attempts. The result is the diffraction pattern in Figure 28.

This first spot pattern has a preferred orientation which indexes to a [1 $\bar{3}$ $\bar{6}$] orientation (beam direction) of GaAs. For a cubic structure, the beam direction is obtained by taking the cross product of any two (hkl) vectors. The error associated with the measurement of spacings between planes and angles between planes is summarized in Table 4. The unusual orientation is a result of tilting of the specimen on the order of 10° off normal to achieve a sharper pattern. Also, the diffraction pattern contains other spots which almost form a ring pattern. This ring pattern also indexes to the lattice constant of GaAs. The polycrystalline quality could be the result of the microtoming process. The significance of this diffraction pattern is that it proves that the darker region is the GaAs substrate.

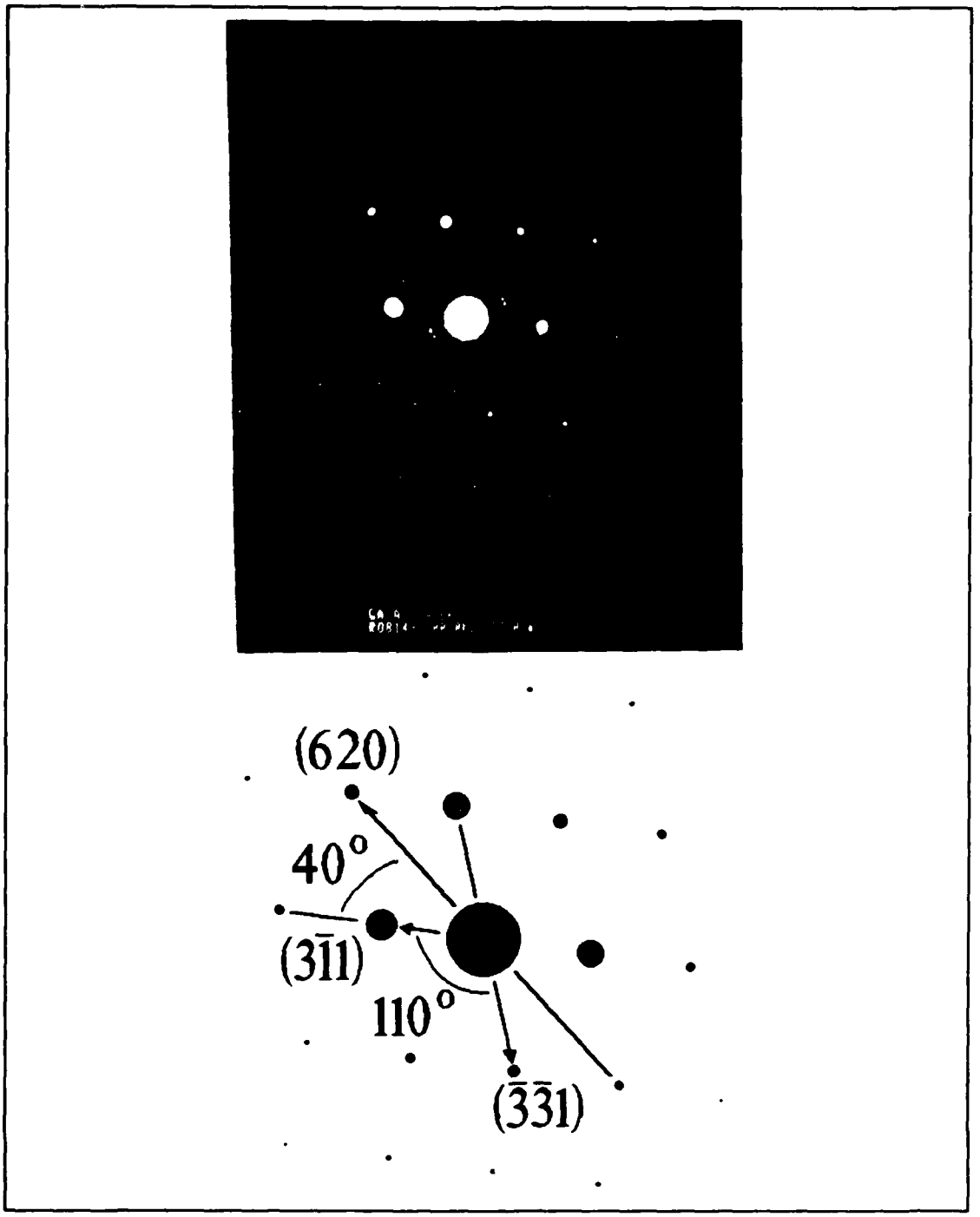


Figure 28. Selected Area Diffraction Pattern of the Lower Interface Region (Area #1) for Sample 3903

Table 4. Error Associated with Indexing Selected Area Diffraction Pattern to GaAs

	d_i Spacings (Å)		
	Measured	Calculated	Error
(6 2 0)	0.8974	0.8939	+0.39%
($\bar{3}$ $\bar{3}$ 1)	1.2917	1.2970	-0.41%
(3 $\bar{1}$ 1)	1.7107	1.7045	+0.36%
	Angles Between Planes		
	Measured	Calculated	Error
(6 2 0), (3 $\bar{1}$ 1)	40.0°	40.3°	-0.74%
($\bar{3}$ $\bar{3}$ 1), (3 $\bar{1}$ 1)	110.0°	110.2°	-0.18%

The second spot pattern shown in Figure 29 is from selected area #2, the lighter region of the bright field micrograph in Figure 26. The surprising result is that this pattern indexes to indium and to a zone axis of [1 0 $\bar{1}$]. Indium is a face-centered tetragonal lattice with a = b = 4.5979 Å and c = 4.9467 Å. The error associated with the measurement of spacings between planes and angles between planes is summarized in Table 5. This is a very significant result because pure indium should not be present anywhere in the interfaces of this material. The possibility that this has anything to do with the indium solder used during MBE growth is discounted. This is because the diffraction pattern is through a cross section, and the selected area is a

specific region of contrast from the bright field image. Furthermore, the indium solder would no doubt be polycrystalline.

Table 5. Error Associated with Indexing Selected Area Diffraction Pattern to Indium

	d_i Spacings (Å)		
	Measured	Calculated	Error
(1 1 1)	2.7280	2.7169	+0.41%
(0 2 0)	2.3250	2.2990	+1.13%
(1 $\bar{3}$ 1)	1.4052	1.3950	+0.73%
	Angles Between Planes		
	Measured	Calculated	Error
($\bar{1}$ $\bar{1}$ $\bar{1}$), ($\bar{1}$ 1 $\bar{1}$)	73.0°	72.4°	+0.83%
(0 2 0), ($\bar{1}$ 1 $\bar{1}$)	53.5°	53.8°	-0.56%

TEM Summary. The preceding analysis does not fully characterize the MBE layers of 3903. However, it does confirm the hypothesis that the layers were unsatisfactory for the purpose of device fabrication. The JEOL 2000FX is also equipped with a standard Tracor x-ray spectrum analyzer. It measures the characteristic x-rays emitted during characteristic energy transitions in a material due to excitation by the electron beam. The observed peaks for Ga and As were strong when analyzing the sample. When the regions which have been analyzed as pure indium were observed,

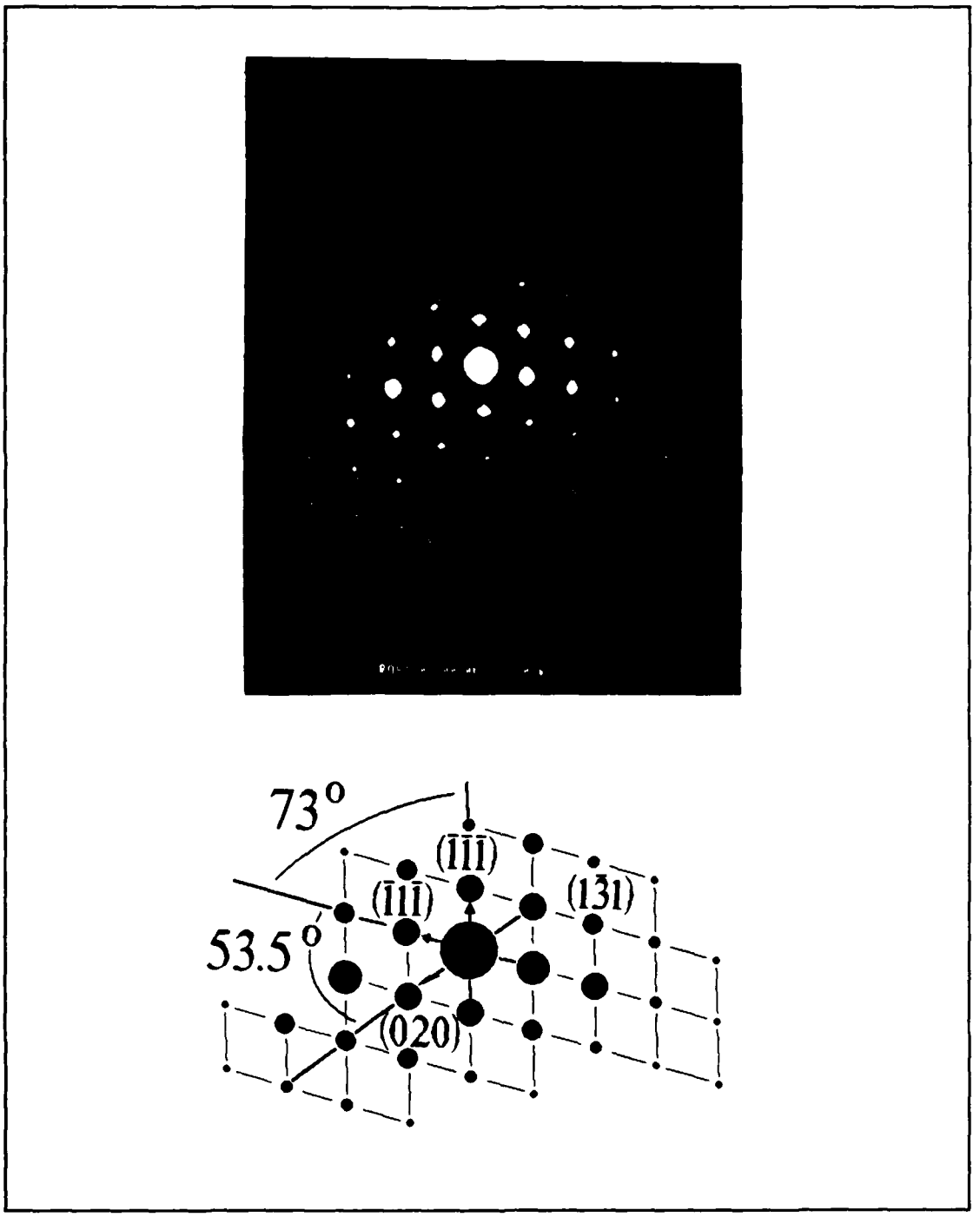


Figure 29. Selected Area Diffraction Pattern of the Upper Interface Region (Area #2) for Sample 3903

the peak for indium became the only one (excluding Cu from the system and Ni from the grid). Another result from the x-ray analyzer was that no aluminum peak (anywhere) in any of the samples was observed. This is perhaps attributable to the problem with the aluminum effusion cell.

Finally, an independent photoluminescence test done at the University of Illinois confirms this conclusion. Photcluminescence is the emission of optical radiation as a result of excitation by optical radiation [60]. This is done at very low temperatures (4 °K) to exclude any radiation that is the result of the temperature of the material. In a quantum well heterostructure, the expected result is a wavelength which correspond to the transition of the band gap of the material where the quantum well is. Thus, for a pseudomorphic structure, one would expect to observe a peak emission near 9100 Å corresponding to the 1.36 eV band gap of $In_{0.15}Ga_{0.85}As$. The result on MBE layer 3903 was that no peak corresponding to this wavelength was observed.

Gate Deposition

The following sub-sections detail and analyze the test results of the gate deposition processes that were performed during this effort. The section is organized according the steps that were taken to: 1) calibrate the process with the profilometer, and 2) fabricate the various devices.

In addition to the growth run designators 3409 and 3903, individual samples were numbered and lettered (e.g. 3409-1,

3903-1A) if necessary because the sample was divided during the fabrication. In accordance with the fabrication procedures described in Chapter III, molybdenum gates were deposited at various thicknesses. For sample 3409-2, the finer 2 μm gates lifted off because the standard photoresist process was used. For subsequent samples, the lift-off was accomplished with the PR hardening chlorobenzene technique described in Chapter III. This process allowed for cleaner lift-off with the thicker depositions. The thicker molybdenum was needed to insure the blocking of the implant.

Table 6. Thicknesses of Molybdenum Gate Depositions

Sample	Gate Thickness (Å)
3409-1	100
3409-2	2075
3409-4	1150
3409-5	1150
3903-1	2050
3903-2	900

Profile Measurements. These gate thicknesses were first estimated with the thickness monitor. The values were then confirmed from profilometer measurements. Table 6 summarizes these measured values for the different fabrication runs. An example of a typical profile measurement after gate deposition is shown in Figure 30.

Cap Layer Etch. A critical step associated with the gate deposition is the self-aligned cap layer (InAs) etch. This liquid etch is necessary to remove what would be a conduction path between the gate and the source or drain. It is a critical step. It is critical because of the ion implantation step which follows. If too much of the AlGaAs is removed with this etch, even a low energy (50 KeV) implant will go too deep into the GaAs buffer layer. This means that the peak of the implant would not contact the 150 Å channel region.

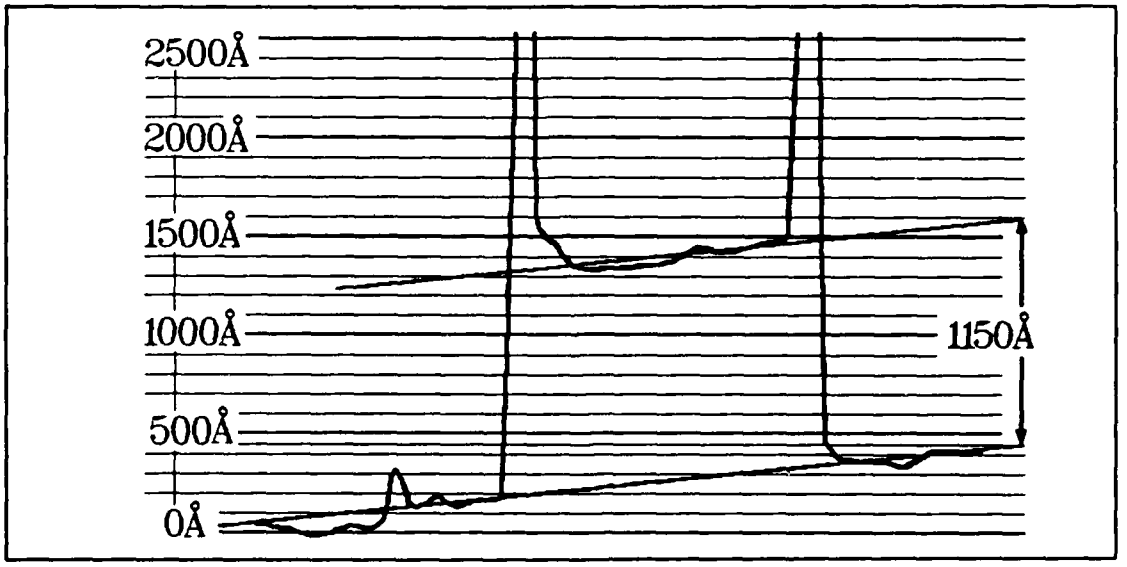


Figure 30. Profilometer Measurement after Gate Deposition for Sample 3409-4

The very first sample (3409-1) did not undergo the cap layer etch because it was felt that the InAs could be used to produce high quality ohmic source and drain contacts. Thus, the cap etch was attempted after the source and drain

deposition. Because of an inordinately high gate leakage current in this device and a concern that this etch might have caused the leakage, successive fabrications included the cap etch right after gate deposition. Table 7 summarizes the results of the cap layer etches as measured by the profilometer.

Table 7. Thicknesses Associated with Capping Layer Etch

Sample	Total Etch (Å)	Cap Thickness (Å)	AlGaAs Thickness (Å)	Remaining AlGaAs (Å)
3409-2	300	200	500	400
3409-4	350	200	500	350
3409-5	350	200	500	350
3903-1	900	500	530	130
3903-2	600	500	530	430

An example of a typical profile measurement after the capping layer etch is shown in Figure 31. From this figure, it is apparent that the etch on 3409-4 resulted in the surface of the structure becoming pitted. Although the mean etch depth is approximately 350 Å from the straight line estimate, the profile reveals that the surface varies by as much as 200 Å in either direction from the straight line estimate. At these dimensions, variations of such magnitude cannot be taken lightly. This cap etch is a critical part in the fabrication process. From the considerations of: gate under-

cutting, depth, and surface consistency, it is important to control this etch.

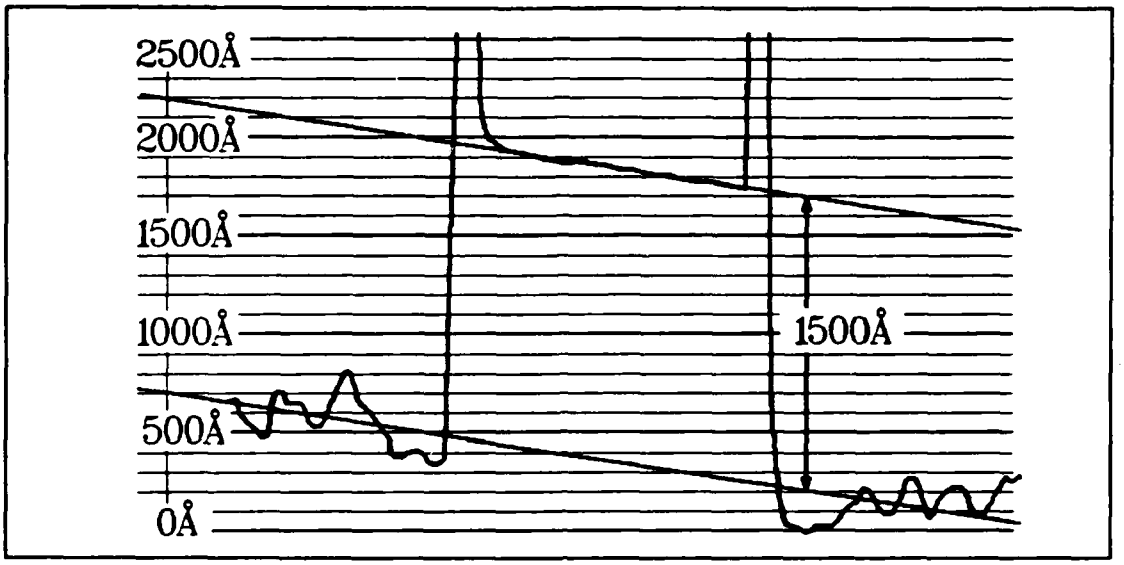


Figure 31. Profilometer Measurement after Cap Layer Etch for 3409-4

However, throughout the different fabrications, control of this etch remained a consistent problem. For sample 3409-2, the following happened. According to both the literature and the experience at CSL, a 1:1:38 solution of H_3PO_4:H_2O_2:H_2O should etch InAs at 20 Å/sec and AlGaAs at 14 Å/sec. Sample 3409-2 was etched for 20 seconds in a 1:1:38 solution which, according to the estimates, should etch the 200 Å of InAs and then 140 Å into the AlGaAs. However the profile revealed that only 200 Å total had been etched. With this sample, no pitting of the surface was observed, and a 1:1:78 solution of H_3PO_4:H_2O_2:H_2O was used for 15 more seconds

to etch 100 Å into the AlGaAs. For sample 3903-1, the opposite happened. This sample was etched for 35 seconds in a 1:1:38 solution which, according to the estimates, should etch the 500 Å of InAs and then 140 Å into the AlGaAs. However the profile revealed that 400 Å (too much) of the AlGaAs had been etched.

Such measurements indicate an inability to control the cap layer etch. This might be due to the difference in the InAs layer thickness or the quality of 3409 versus that of 3903. However, the surface pitting problem observed in 3409-4,5 was not observed in 3409-2 or 3903-1,2. Inconsistent etching practices or solutions could also yield such lack-luster results. In general, despite attempts to change concentrations and exercise consistent procedures, the cap layer etch remained an unpredictable process throughout the various fabrications.

Ion Implantation

The following sub-sections detail and analyze the test results of the ion implantation processes that were performed during this effort. This section is organized according the experimental steps that were taken to: 1) calibrate the process, and 2) fabricate the various devices.

Calibration. The purpose of this step was to find appropriate implantation conditions for the ion implanter at AFWAL. In order to determine an appropriate energy and dose for the SISFET fabrication, three samples of MBE grown,

undoped GaAs were implanted under different conditions. An underlying assumption here is that implanting into GaAs produces results similar to implanting into the hetero-structures of the SISFET. All three samples were implanted with ^{+28}Si ions at a dose of 1 x 10^{13} ions/cm^2. This flux was chosen because it produces a predicted (LSS) peak concentration on the order of 10^{18} cm^{-3} in GaAs. The energies used were 60, 100, and 180 KeV. The samples were annealed between silicon wafers at 800 °C for 15 seconds in the Rapid Transit Anneal (RTA). Capacitance-Voltage (C-V) and Secondary Ion Mass Spectroscopy (SIMS) were done. The range (depth into the sample of peak concentration) and peak concentration for these various energies were estimated from the C-V and SIMS graphs. The results are shown in Table 8 along with the LSS predicted value taken from a computer model at AFWAL [34].

Although the various numbers are not in perfect agreement, they provided the estimates necessary to proceed with the fabrication attempt. With the proposed SISFET structure, the ideal implant profile has a peak at or very close to the AlGaAs/InGaAs heterointerface (or channel). The reasons for this are: 1) to provide maximum carrier concentration in the channel, and 2) to reduce the potential for parasitic conduction by inadvertently doping the GaAs buffer layer.

Assuming an optimum cap layer etch, there remains approximately 400 Å of AlGaAs. This means that an implant

Table 8. Implant Range into GaAs and Peak Concentration at a Dose Equal to 1 x 10^{13} ions/cm^2 Measured by C-V and SIMS

Implant Energy	C-V	CSL SIMS	AFWAL SIMS	LSS (pred.)
		RANGE		
60 KeV	850 Å	800 Å	500 Å	500 Å
100 KeV	1000 Å	950 Å	800 Å	900 Å
180 KeV	1900 Å	1900 Å	1800 Å	1700 Å
		PEAK CONCENTRATION (cm^{-3})		
60 KeV	$2.5x10^{17}$	$9x10^{17}$	$4x10^{17}$	$1.5x10^{18}$
100 KeV	$4x10^{17}$	$7x10^{17}$	$6x10^{17}$	$6x10^{17}$
180 KeV	$3.5x10^{17}$	$3x10^{17}$	$2x10^{17}$	$6x10^{17}$

peak need not go further than approximately 500 Å (400 Å of AlGaAs and 100 Å of InGaAs) into the structure in order to contact the channel. The data presented above made manifest that an implant energy of 50 KeV to 60 KeV would suffice. Implant energies less than 50 KeV were not possible because the Varian 400-10A will not operate stably below this energy. Also, the data in Table 8 made evident that a dose of 1 x 10^{13} ions/cm^{-2} would not yield a doping concentration of 10^{18} cm^{-3}. Therefore, all implant doses for SISFET fabrication were 5 x 10^{13} ions/cm^{-2} in order to achieve a peak concentration closer to 10^{18} cm^{-3}. Another result here is that the C-V measurement yielded values of peak concentration close to

those from SIMS. This indicates an efficient activation of the implanted ions into the lattice sites. This is true because the C-V technique measures the carrier profile by measuring the reverse bias capacitance. Thus, it can only measure a profile that is an electrically active profile.

Fabrication. The test parameters used for the ion implantation that was done to fabricate SISFETs are shown in Table 9. All implants for fabrication were done with a dose of 5×10^{13} ions per cm^2. Energies were varied in an attempt to achieve an implant profile peak at or near the channel region. The orientations of 3409-1 and 3409-2 in the implant chamber were not considered. Subsequent samples were tilted off normal to (100) along the gate widths of the smaller FETs. As defined in Appendix A, this involved a rotation about the x axis. This ensured that the tilt would not produce an implant unsymmetric about the gate on the source/drain sides of the gate.

Annealing

The following sub-sections detail and analyze the test results of the annealing processes that were performed during this effort. The section is organized according the experimental steps that were taken to: 1) calibrate the process using control samples, and 2) fabricate the various samples under different conditions.

Calibration. Various steps were taken to insure the validity of the annealing process. One of the outcomes of a

Table 9. Ion Implantation Test Parameters Used During Fabrication of SISFET Structures

Sample	Energy (KeV)	Dose (cm^{-2})	Angle (°)
3049-1	60	5×10^{13}	7
3409-2	100	5×10^{13}	9
3409-4	60	5×10^{13}	7
3409-5	60	5×10^{13}	7
3903-1	50	5×10^{13}	7
3903-2	50	5×10^{13}	7

Monolithic Microwave Integrated Circuits (MMIC) implant study done at AFWAL is a technique for evaluating the condition of the RTA thermocouple. This is done with GaAs samples that are dual implanted: 130 KeV at 3×10^{12} cm^{-2} and 50 KeV at 0.7×10^{12} cm^{-2}. These samples, which are identical to those used in the MMIC study, were annealed at the same time and temperature which, in the MMIC study, produced a mobility of 3750 $cm^2/(V \cdot s)$ and an activation of 45% [7]. The results of this MMIC study, from Hall mobility measurements, are summarized in Table 10.

The following process was done prior to most of the annealing done during fabrication in this study. First the dual implanted GaAs sample was subjected to 30 second rinses in trichloroethylene, acetone, methanol and isopropyl in that order. The sample was then blown dry with N_2 gas. Next the

Table 10. MMIC Study Results for Mobility and Activation of Dual Implanted GaAs Annealed at Various Temperatures for 10 Seconds in the Heatpulse 210T at AFWAL

Temperature (°C)	Mobility ($cm^2/(V \cdot s)$)	Activation (%)
825	1550	74
850	3625	49
875	3500	50
900	3700	44
925	3350	34

sample was: etched in a $HCl:H_2O$ (1:1 by volume) solution for 1 minute, rinsed in DIW for 5 minutes, etched in a Buffered Oxide Etch (BOE) for 1 minute, rinsed in DIW for 10 minutes, and then dried in a N_2 oven at 100 °C for 5 minutes. These steps created a clean oxide-free surface prior to annealing. The sample was then annealed between two silicon wafers for 10 seconds at 900 °C in an atmosphere of forming gas. Following the anneal, four point probe measurements were taken. A measurement of 620 Ω/■ with a standard deviation of not more 95 Ω/■ confirmed proper operation of the thermocouple. If results are achieved outside the range 525-715 Ω/■ (± 2 standard deviations), then experience at AFWAL

indicates that either the thermocouple needs to be replaced or the RTA chamber needs cleaning.

An additional experiment was done because of a concern that the temperature of the sample might be considerably different than the temperature indicated by the ThermoCouple (TC) installed and embedded in the silicon baseplate of the RTA. An additional Omega CHAL-005 Chromel-Alumel TC was installed into the RTA in a setup identical to that used for the device fabrication annealing. This is shown in Figure 32.

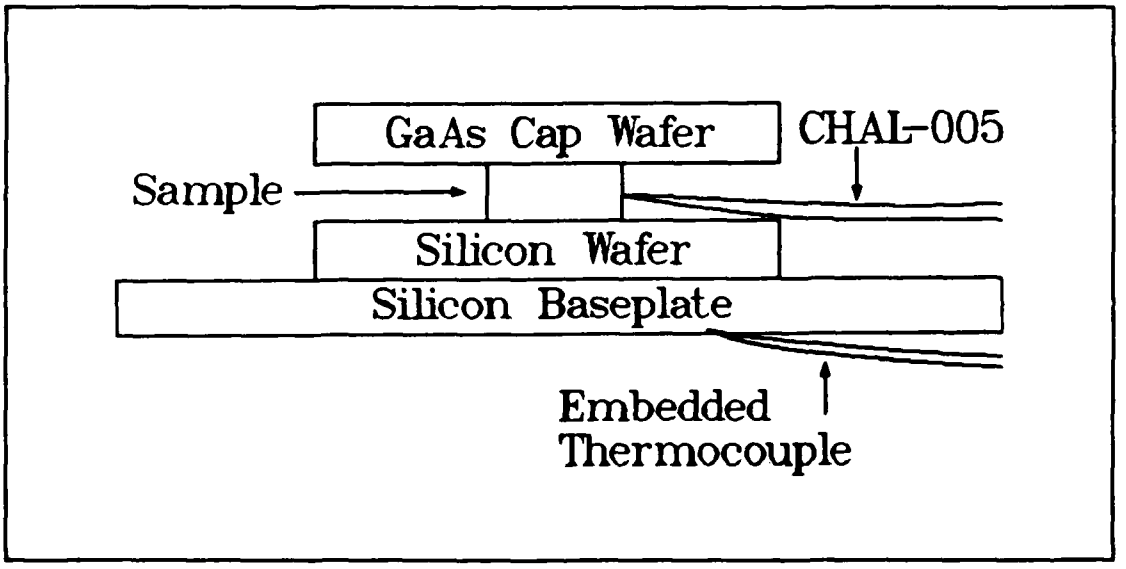


Figure 32. Arrangement During Annealing with Additional Thermocouple Touching Sample. Both Thermocouples were Type-K Chromel-Alumel of Similar Diameter

The CHAL-005 TC was connected to a standard Chromel-Alumel (Type-K) TC reader, and was installed into the Heatpulse 210T RTA chamber. The leads were insulated around

the RTA chamber door in order to keep them from shorting. The CHAL-005 is 0.005 inch diameter wire that can withstand long term exposure to temperatures up to 1100 °C. The thermocouple was placed, as shown in Figure 32, so that it touched the GaAs sample. The sample was annealed at 900 °C for 10 seconds.

The result was that the reading on the CHAL-005 TC increased faster than that of the originally installed TC. However, during the whole annealing cycle, the reading on the CHAL-005 was always within 30 °C of the reading on the original TC. At the peak of the anneal, the CHAL-005 peaked at 928 °C, and then it cooled off slightly faster than the original TC as well. A more accurate test could have included either embedding or cementing the TC to the sample. However, this test, which was done only once, provided additional confidence that the originally installed TC was reasonably accurate. More importantly, it confirms that the samples annealed during fabrication were subjected to temperatures reasonably close (well within 50 °C) to the temperatures indicated by the originally installed thermocouple.

Fabrication. The test parameters used for the annealing that was done to fabricate SISFETs are shown in Table 11. Samples 3409-1A and 1B were proximity annealed between two silicon wafers. Subsequent samples were proximity annealed under a GaAs cap wafer as described in Chapter III. All samples were annealed using the automatic thermocouple mode because the process with this mode is very repeatable.

Table 11. Test Parameters Used for Rapid Transit Annealing During SISFET Fabrication

Sample	Anneal Temperature (°C)	Anneal Time (sec)
3409-1A	650	25
3409-1B	700	25
3409-2	800	2
3409-4	800	2
3409-5	800	2
3903-1A	800	10
3903-1B	800	15
3903-1C	825	5
3903-1D	850	5
3903-1E	875	5
3903-2	800	10

Source and Drain Deposition

The following section presents the results of the source and drain depositions. This whole process including the alloying, as described in Chapter III, is very straightforward. Therefore, it is highly unlikely that the processing during this step contributed to device failure. The greatest potential for error in this step is during the optical lithography (alignment) process. Because the gates are already deposited, the spacing between the gate and the

source and drain contacts is determined here. However, good alignment was achieved in all cases. This was easy to observe under an optical microscope even before developing the photoresist. The exact thickness of source and drain depositions from each fabrication, as measured by the profilometer, are very close. Typical depositions were 400 Å of AuGe, 100 Å of Ni, and 600 Å of Au. The devices and TLM patterns were probed right after the deposition, but no good characteristics were ever observed until the samples were alloyed.

Alloying. During this process it is expected that the germanium will diffuse down into the implanted region and produce an ohmic contact. The results of alloying are as follows. As observed under an optical microscope, none of the 3409 samples consistently alloyed. When a contact alloys (diffuses) its surface becomes irregular. Inconsistent alloying can be attributed to not having a regular lattice structure underneath. Since the annealing times for the 3409 samples were very low, it is likely that annealing did not sufficiently repair the damage from ion implantation. This is consistent with not observing good ohmic contacts, as will be described in the next section. Sample 3409-4 was alloyed twice and then a third time at 550 °C for 60 seconds in an attempt to allow more time and higher temperature for the germanium to diffuse. The contacts appearance or electrical characteristics did not change. After source and drain

deposition, the 3903 samples were also non-ohmic. The alloying was not as inconsistent, and it did produce ohmic contacts occasionally. It is believed that the higher temperatures and longer times during rapid transit annealing were a major factor.

Finished Samples

The following sub-sections detail and analyze the results of the tests that were performed during this effort to characterize the finished samples. The section is organized according the experimental steps that were taken to: 1) examine the surface properties and dimensions, (2) measure the specific contact resistance, and 3) measure the I-V characteristics of the various samples.

SEM Analysis. A series of SEM micrographs were taken in order to verify the dimensions and surface properties of the fabricated devices. The two pictures in Figure 33 show one of the transistors from sample 3409-4. This one has a 10 μm gate length and 100 μm gate width. The observed dimensions are exactly the same as the expected dimensions. These particular source and drain contacts have a good alloyed appearance. Furthermore, the result of the mesa etch is visible.

The next two micrographs in Figure 34 are of the same device but at a much higher magnification. These pictures show the edge of the molybdenum gate in the active region. The pitting of the surface resulting from the cap layer etch

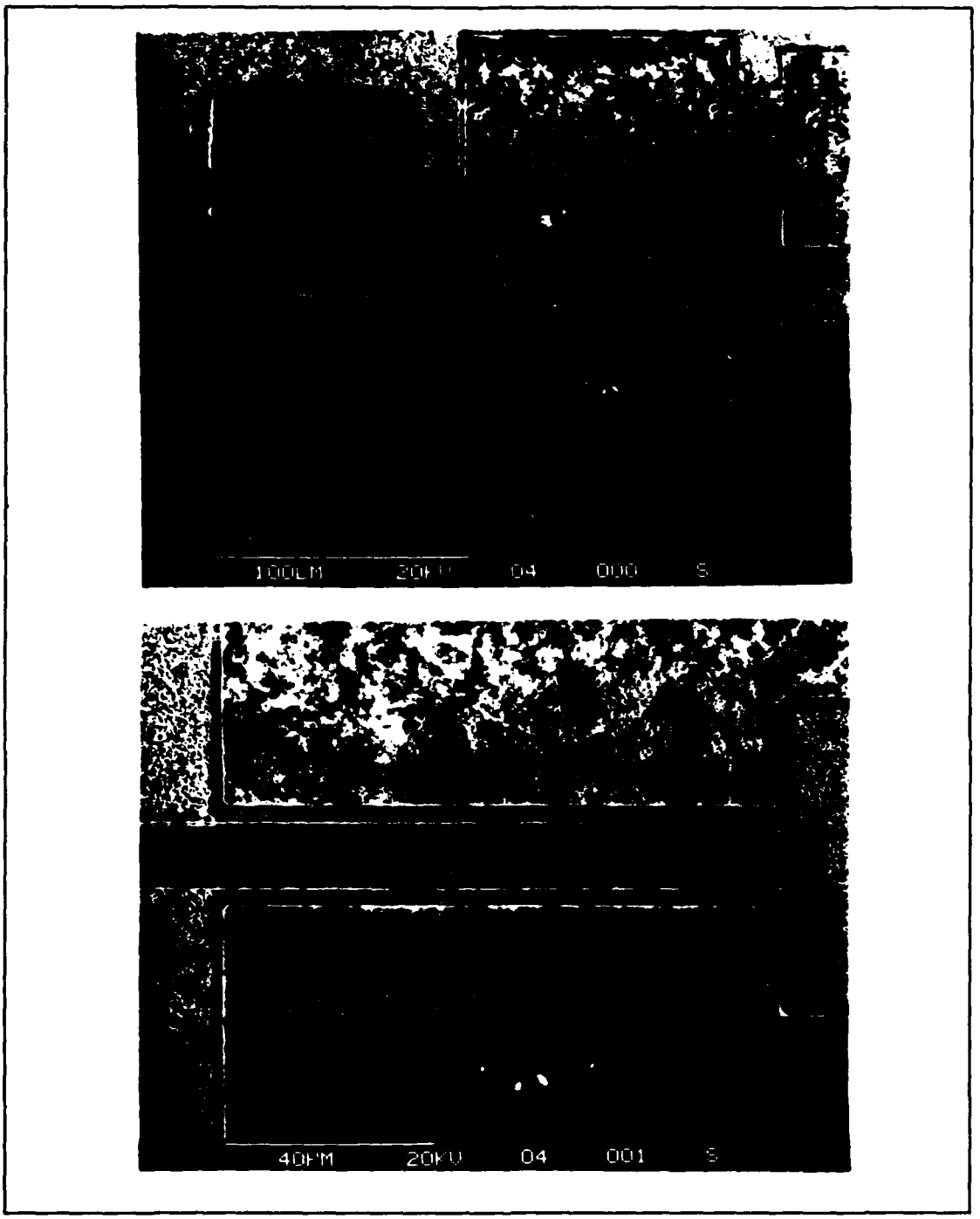


Figure 33. SEM Micrograph of a 10 x 100 μm Gate Transistor on Finished Sample 3409-4. Alloying and Mesa Isolation are Visible.

is confirmed. Due to a glitch in the SEM, the scale on the picture incorrectly reads 0 μm. The top picture has a 2 μm scale and the bottom picture has a 1 μm scale. The picture shows that the cap layer etch has undercut the gate by 0.8 μm on each side. Furthermore, the undercutting has resulted in the gate metal shearing off and dropping away. In the case of 3409-4, the gate leakage was very low. Therefore, this effect is not the cause of the gate leakage. However, this artifact indicates a considerable amount of undercutting, and it explains why many of the finer 2 μm gates practically disappeared.

The next four pictures in Figure 35 and Figure 36 reveal a problem with using a MODFET mask set to build a SISFET. The mesa mask only covers the active region because in a MODFET fabrication, this is the first step. For the SISFET, the gate deposition is the first step. This means that during the mesa etch, neither the gate pad or the finger of the gate which extends beyond the active region are protected. The top picture shows the severe undercutting of the gate pad which results. The bottom picture shows a top view of the gate finger beyond the active region. The undercutting is visible here. The two pictures in Figure 36 show the gate finger undercutting in greater detail. Both pictures reveal that at this end of the gate, the molybdenum is actually starting to curl up where it has been undercut by the mesa etch. The scale of the upper picture in Figure 36 is 2 μm.

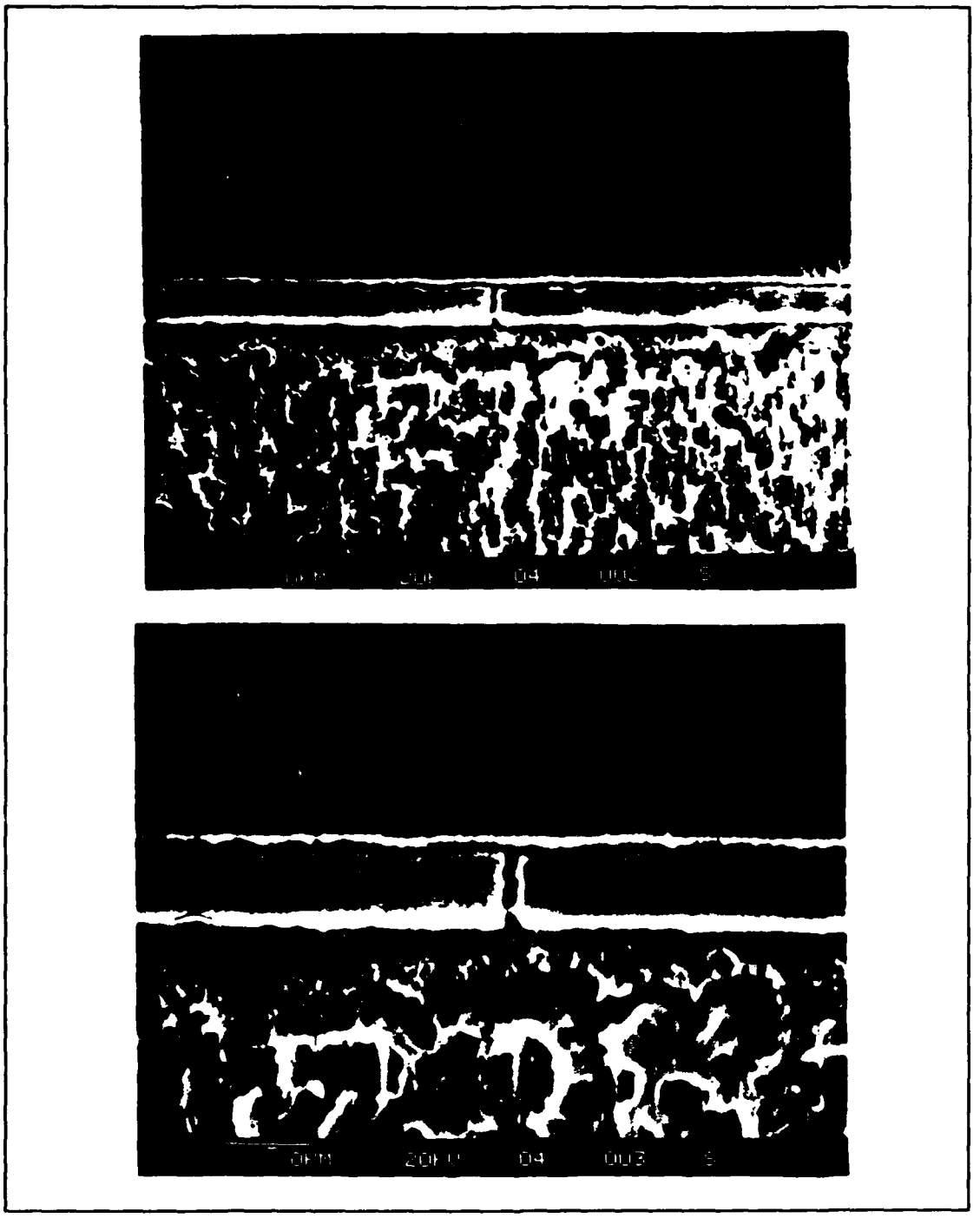


Figure 34. Magnification of Gate Area of Same Transistor. Pitting, Undercutting, and Shearing are Observed

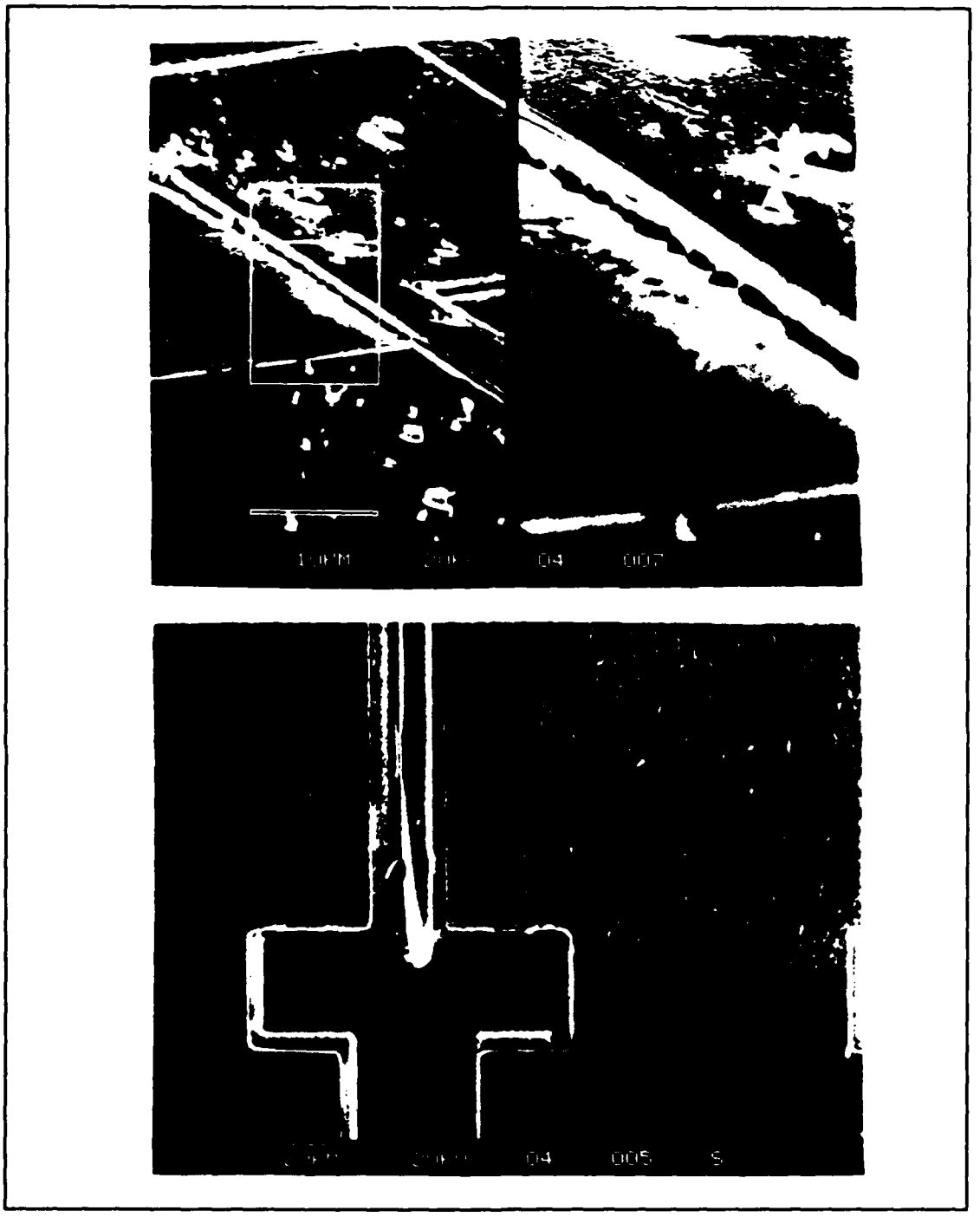


Figure 35. SEM Micrographs Showing Undercutting of Unmasked Gate Regions During Mesa Etch.

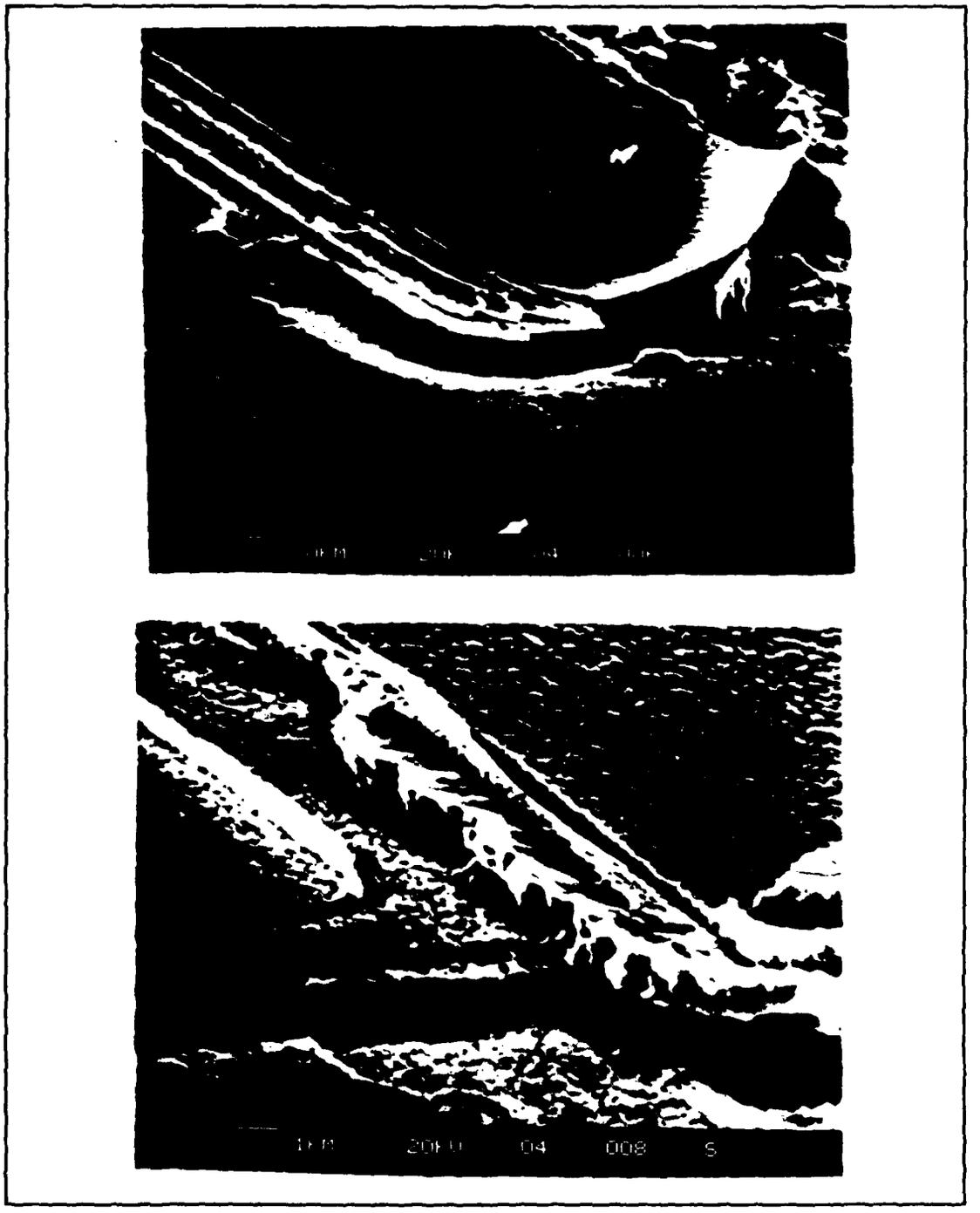


Figure 36. Magnified View of Gate Finger Undercutting Caused by Mesa Etch

Specific Contact Resistance. With samples 3903-1 and 3903-2, reasonable and consistent numbers were obtained for specific contact resistance. The Transmission Line Method (TLM), which is illustrated in Figure 37, was used to measure these values. During source and drain deposition sets of 75 μm wide contact pads, separated by spaces of 1, 2, 3, 4, 6, 8, and 10 μm, were deposited on the implanted AlGaAs regions of every sample. The samples were placed on the AFWAL microprobe station connected to a Keithley Instruments (KI) 225 constant DC current source. A Hewlett-Packard 3465B digital multimeter was connected in parallel to the samples as shown in Figure 37. A fixed current of 500 μA was passed through the contact pairs in the TLM pattern, and the voltage between the contacts was measured with the multimeter. Ohm's Law gives the resistance.

The result is an excellent linear fit of resistance vs. contact spacing. The arrangement of using both the current source and the multimeter allows for removal of the error associated with measuring small resistances. Both the current source and the multimeter have a non-infinite input impedance. Much of the error associated with each unit and with the resistance of the leads is cancelled out during the Ohm's Law division. The resistance versus contact spacing data was fit to a degree one (linear) curve. The ordinate intercept of the resultant line is the theoretical point where the contact spacing is zero. This value is the resistance associated just

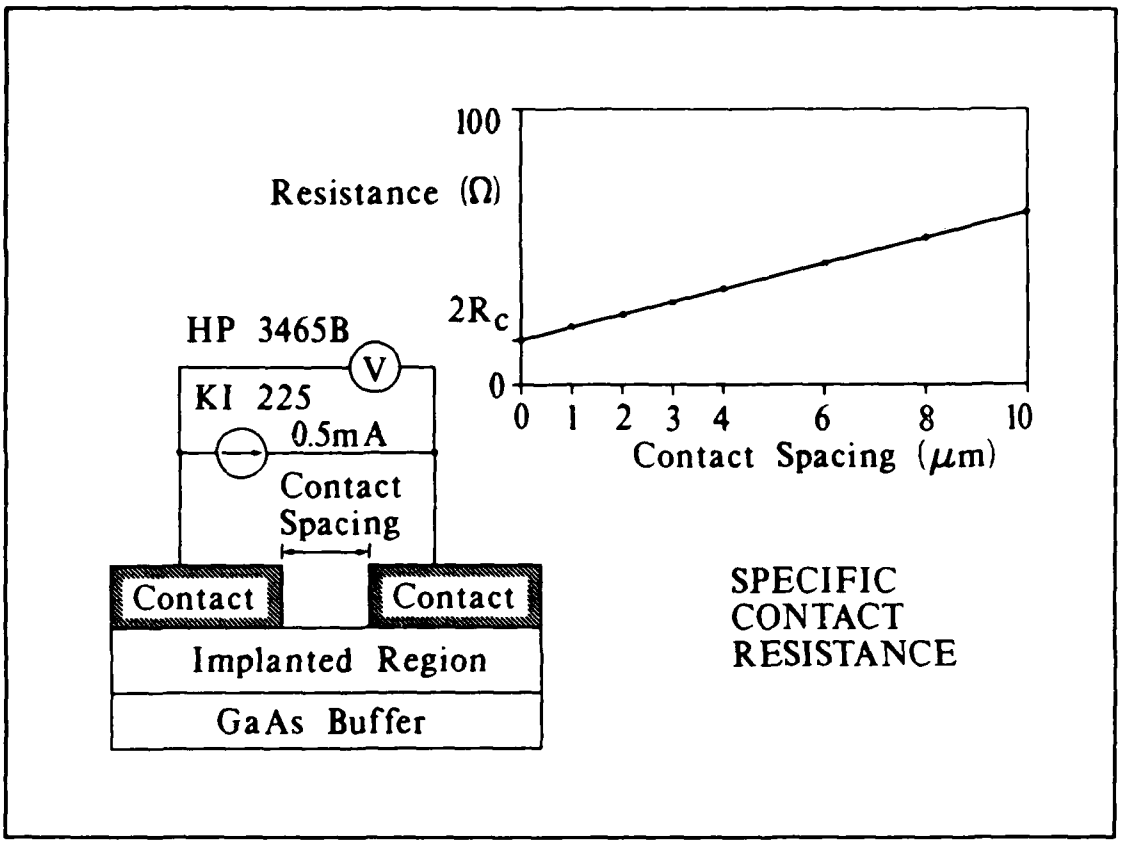


Figure 37. Specific Contact Resistance Measurement Technique and Linear Curve Fit [35:100]

with the two contacts and not with any semiconductor material in between. Dividing this value by two and multiplying by the contact width gives a contact width independent (scaled) value for the specific contact resistance, R_c, in units of $\Omega \cdot mm$.

The results from samples 3903-1A through 3903-1E and 3903-2 are summarized in Table 12. The sheet resistance ($\Omega/\blacksquare$) of the semiconductor material under the contact is given by the slope of the line fit to the data. Sheet resistance is a function of the mobility and implant profile of the material

underneath and of the junction depth. It is generally related to the average conductivity of the material when multiplied by the junction depth [59]. The correlation coefficient (ρ) has been calculated according to standard probability theory [9:258] for linear regression. The lower correlation coefficients are the result of a wider variation of R_c when measured over a number of TLM patterns.

Table 12. Measured Specific Contact Resistances Using TLM Method after Alloying 50 sec in H_2 at 500 °C

Sample	R_c ($\Omega \cdot mm$)	R_s ($\Omega/\blacksquare$)	n	ρ
3903-1A	0.65	365	31	0.97
3903-1B	1.75	378	7	0.99
3903-1C	1.58	474	6	0.99
3903-1D	0.93	302	30	0.75
3903-1E	0.77	273	21	0.47
3903-2	1.98	598	28	0.85

All of the 3409 samples exhibited non-ohmic contacts. Specifically, instead of resistances on the order of tens of ohms or less, direct probing revealed resistances on the order of many kilo-ohms or more. In some cases, the values were in the mega-ohm range or among TLM contacts on the same sample, diode characteristics were observed. Specifically, the results for sample 3409-2 were inconsistent. For the other

3409 samples, attempts to measure the specific contact resistance from TLM patterns resulted in non-linear plots. Attempts to condense such data to a least squares fit resulted in negative values of specific contact resistance. This, of course, is an unreasonable result with no significance. It is probable that layer 3409 was the result of good quality MBE growth and that it met the growth specifications. This is because transistor action was achieved with both 3409-1 and 3409-4. Not achieving good results is attributable to not achieving good source and drain contacts, which is attributable to either improper implantation or annealing conditions or both.

The operation of the SISFET relies on an ohmic contact gate as well as ohmic source and drain contacts. Another interesting result came from a control sample that was processed during the gate deposition of 3409-4. A piece of 3409 was exposed to the contact mask (with the TLM patterns) and then developed. Molybdenum was evaporated onto it and then lifted off as described in Chapter III.

The expected result of very low resistance contacts was not obtained. Instead, although the contacts were ohmic in the sense that their I-V characteristic was linear, the resistance was on the order of kilo-ohms. Measured values were 27.3 Ω·mm for the specific contact resistance and 2730 Ω/■ for the sheet resistance. Thus, even though 3409-4 exhibited transistor action, the lack of low resistance, ohmic

source and drain contacts was not the only problem. Further investigation into the specific contact resistance of molybdenum onto heavily doped (5×10^{18} cm^{-3}) InAs was not done. Previous studies have shown that contacts onto n^+-InAs should be quite good, and that the Fermi level should actually be above the conduction band in the InAs [47]. However, the control sample measurements indicate that the assumption of a low resistance gate contact was potentially unwarranted. Because of the problems with MBE crystal growth and potential problems with ion implantation and annealing, it is not clear exactly what this affect had on device performance.

I-V Characteristics. To the extent possible, I-V characteristics were obtained for the various finished samples. Transistor action was obtained with 3409-1; however, gate leakage was a problem. Typical gate diode characteristics are shown in Figure 38. They were obtained from one of the 10 by 100 μm gate transistors (length by width). The drain to source current at saturation was very small (on the order of micro-amps), and the gate leakage was inordinately high.

In analyzing this result, several factors must be considered. First, because only 100 Å of molybdenum was evaporated for the gate, it is likely that either because of thinness or non-uniformity, that the molybdenum did not block the implant. Such a possibility easily explains the high gate leakage. Second, as mentioned before, the cap etch was the

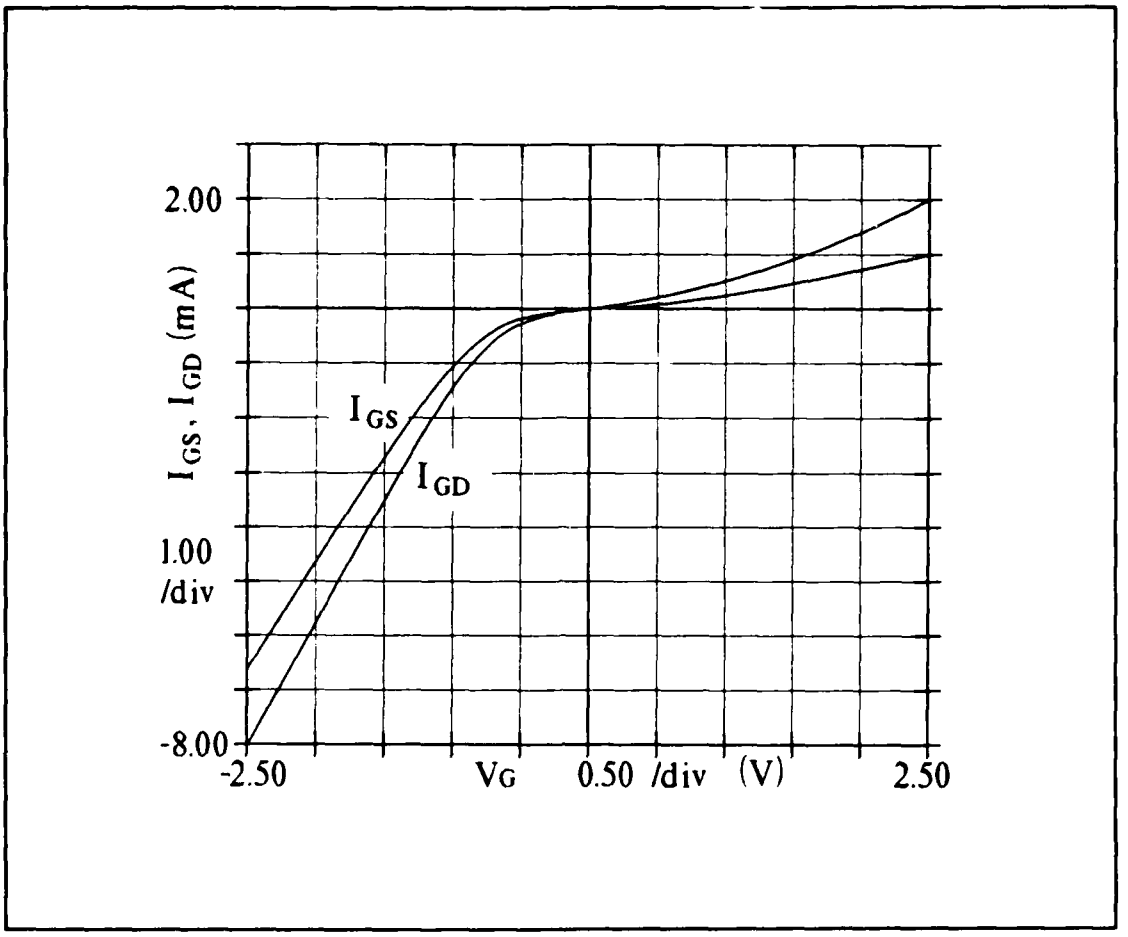


Figure 38. Typical Gate Diode Characteristic for Sample 3409-1, V_{DS} = 0 Volts

last step in the fabrication of this sample. It is possible that uneven wetting caused an incomplete etch of the InAs, even though profile measurements showed a total etch of 350 Å. This could also explain the gate leakage. Third, the low current levels are certainly, at least in part, due to the fact that low resistance source and drain contacts were not

achieved. High source resistances have a direct impact on the current carried by the device.

The characteristics of sample 3409-2 were inconsistent and unmeasurable. No I-V curves are presented for this sample. No saturation characteristic was even observed. There was no gate leakage, but the "devices" just operated as resistors. Applied gate voltage had no effect, and current levels were generally in the micro-amp range. From attempted TLM measurements, the contacts were either non-ohmic or high resistance. During the mesa etch of this sample, examination of the surface with an optical microscope revealed a cracked appearance all over the sample. This was unexpected. The behavior of the finished sample is attributed to the possibility that the layer became polycrystalline. Perhaps, the combination of the higher energy (100 KeV) implant with improper annealing was responsible.

The designation for sample 3409-3 is perhaps conspicuously absent from the discussion. This was an attempt to fabricate the device by using MBE re-growth after a self-aligned etch into the buffer layer. No good results were obtained with this technique, and it is beyond the scope of the effort.

Transistor action was obtained with sample 3409-4. The family of I-V curves for both negative and positive gate bias are shown in Figure 39. These curves were typical. They were obtained from one of the 4 μm by 100 μm gate transistors

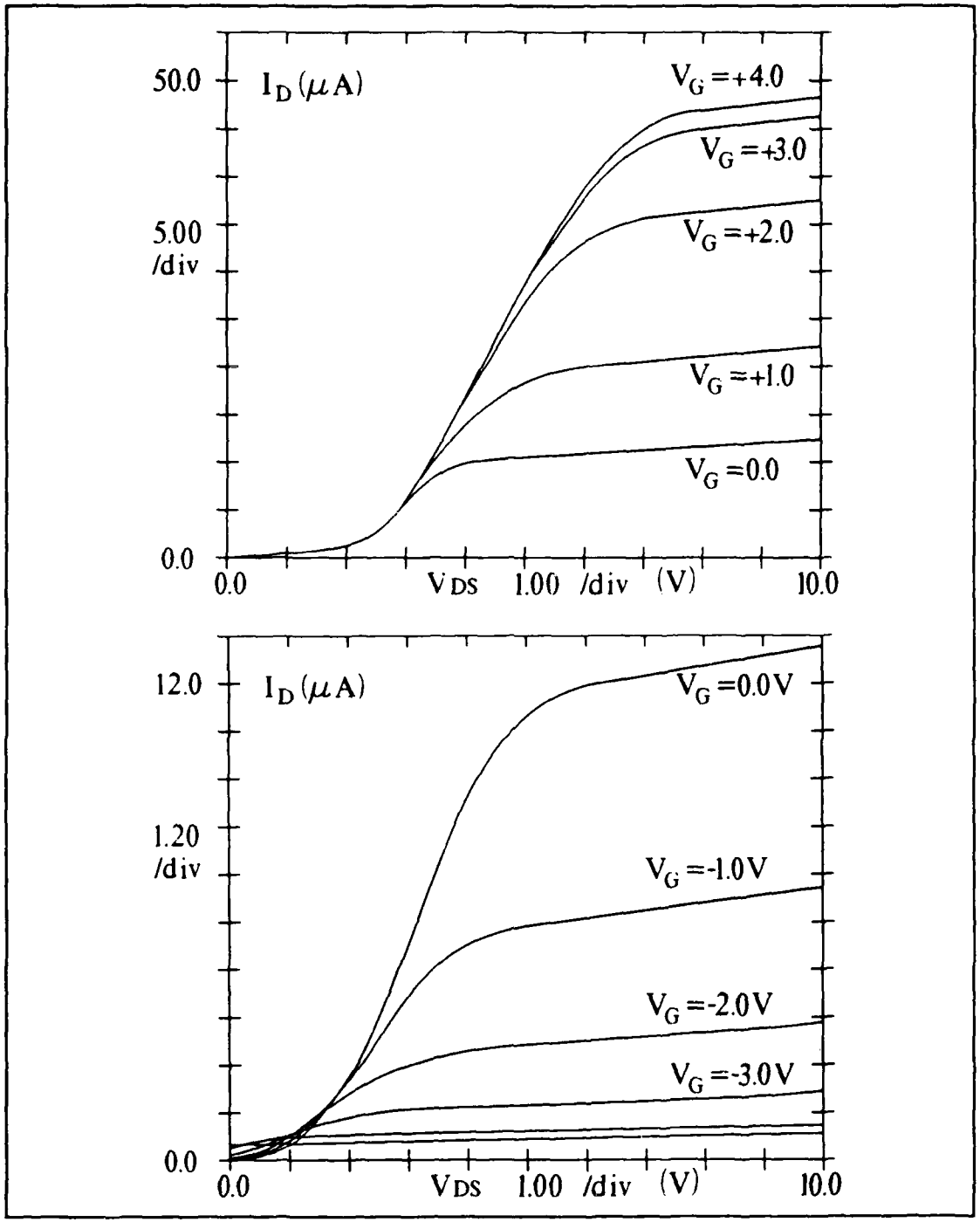


Figure 39. Typical Family of I-V Curves for Sample 3409-4 for Both Negative and Positive Applied Gate Voltage

(length by width). The drain to source current was very small and on the order of micro-amps. The gate diode I-V characteristics are shown in Figure 40. In this case, although the I-V characteristics are similar to those of 3409-1, the gate leakage was very low and on the order of micro-amps.

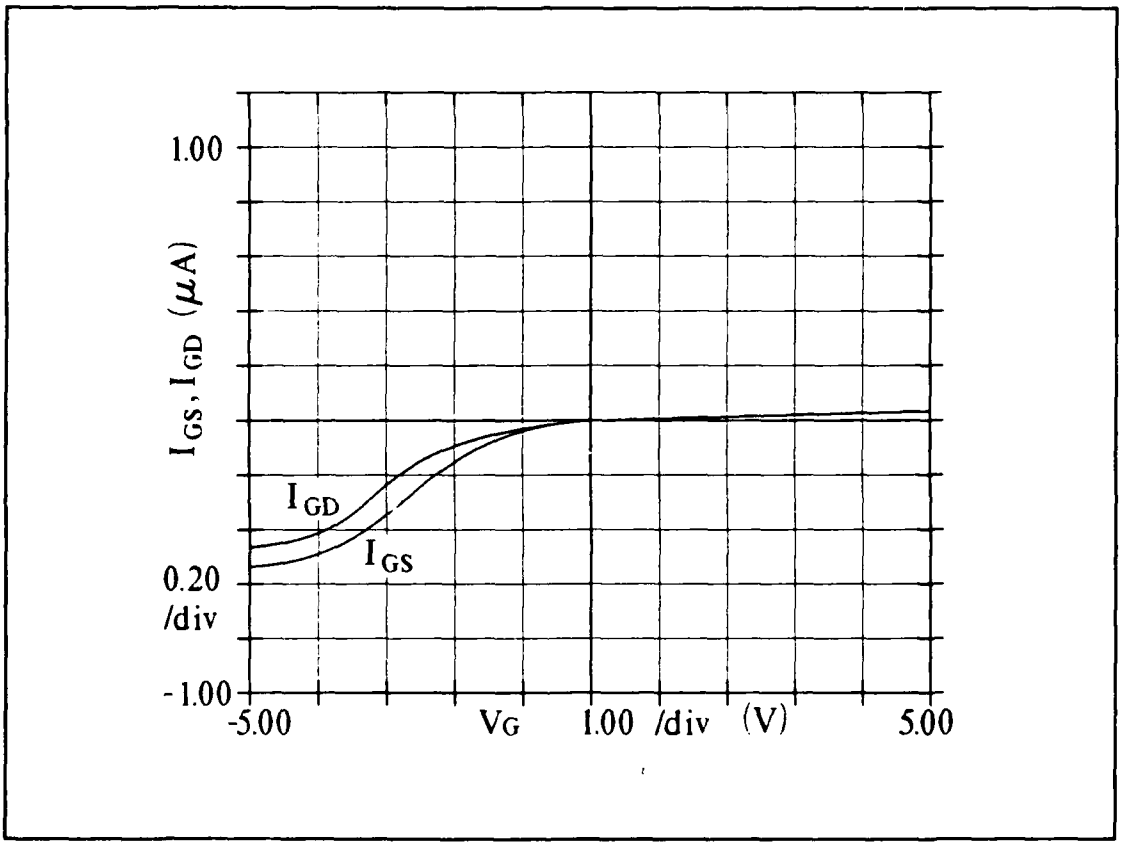


Figure 40. Typical Gate Diode Characteristic for Sample 3409-4

The I-V results of the 3903 samples are as follows. No transistor action was achieved; however, this is attributed to the fact that the MBE layers were bad. The gate diode

characteristics for 3903-2 are shown in Figure 41. The first plot was done before alloying, the second plot after alloying. The data is presented to show the fact that in the case of the 3903 layers, the alloying did have an affect. The affect was not only to produce ohmic contacts, but also that gate leakage in the forward bias direction became larger than in the reverse bias direction. The meaning of the shift is unclear because of the bad MBE growth. However, the result of higher leakage in the forward bias case is what one would expect for a properly fabricated SISFET.

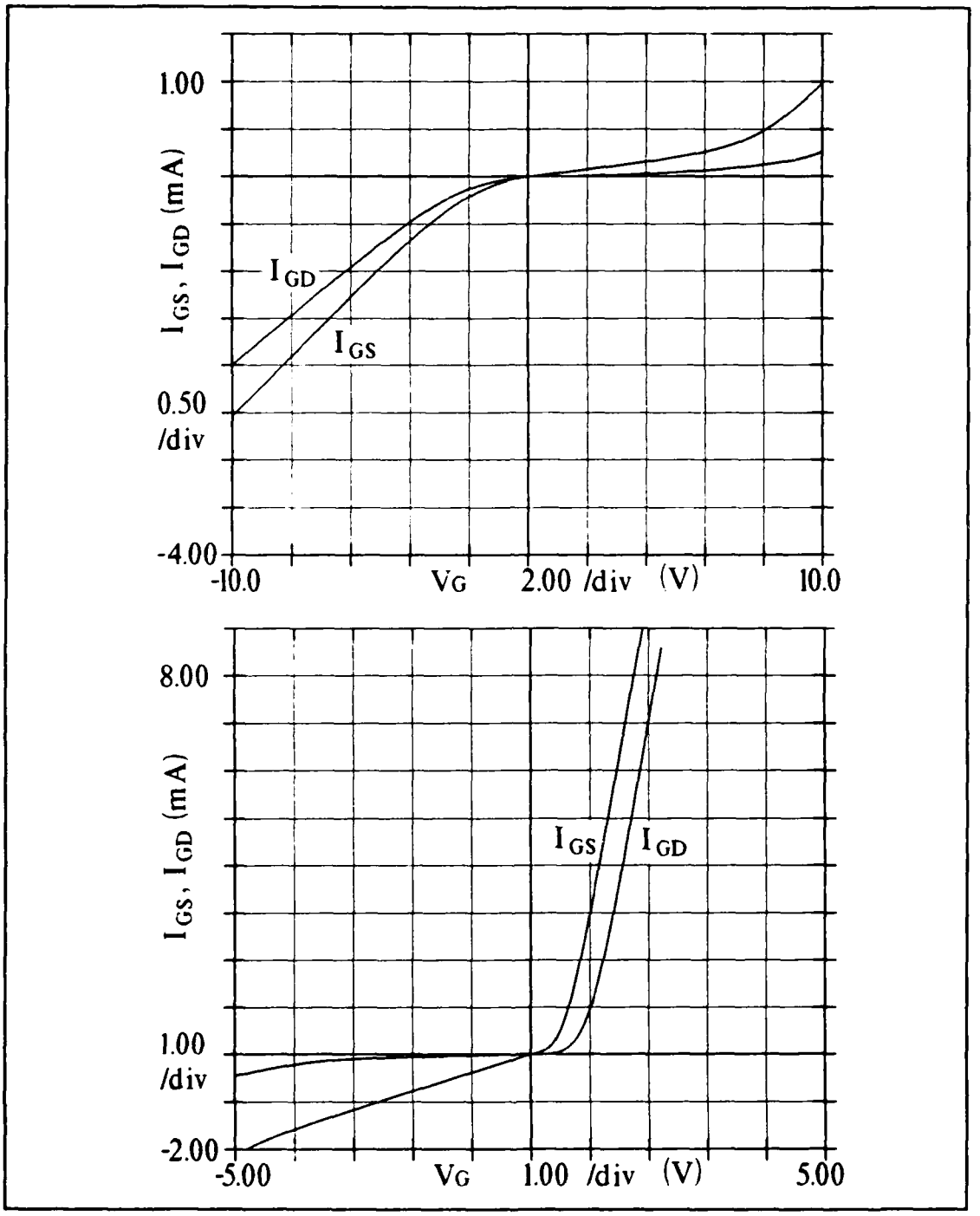


Figure 41. Gate Diode Characteristics of Sample 3903-2 Before Alloying (top) and After Alloying (bottom)

V. Conclusions and Recommendations

This study was an investigation into the concept and fabrication of a pseudomorphic or strained-channel SISFET. The model developed in this study provided the foundation for pursuing the fabrication of this novel transistor structure. In principle, this device solves the problems of process sensitive threshold voltages and limited gate voltage swings in the MODFET. Furthermore, calculations from the model predict superior characteristics (two to three times the barrier) for gate leakage as compared to the standard GaAs/AlGaAs/GaAs SISFET. Thus, the pseudomorphic structure will support gate voltages to three volts. The "natural" threshold voltage is positive, which would be applicable to high speed logic circuits. Also the self-aligned method of fabrication using ion-implanted source and drain regions would also result in a shorter and minimal channel lengths.

Conclusions

The results of characterizing and analyzing the fabrication of the pseudomorphic SISFET are as follows. Because the proposed SISFETs did not operate as expected, these conclusions are stated in terms of the problems encountered with the fabrication. However, the results should not deter further research. In fact, the results of this effort should continue to motivate the investigation of the pseudomorphic SISFET.

1. The MBE growth of layer 3409 may be assumed to have met the specifications for the proposed heterostructure. The reasons for this assumption are that transistor characteristics were achieved and gate leakage was low. The only obvious problem with sample 3409-4 was the lack of good (low resistance) contacts.

2. However, the MBE growth of layer 3903 was definitely defective, and was the primary reason for not getting better results during this effort. This conclusion is supported by a number of qualitative and quantitative factors. These included physical appearance and (after-the-fact) discovery of calibration problems with the Riber 1000 MBE machine. Quantitatively, TEM electron diffraction shows (within 1% of error) pure indium as one of the interfaces in the structure. Furthermore, an independent test done at the University of Illinois shows a flat photoluminescence response.

3. The assumption that molybdenum on heavily doped n^+ InAs results in a very low resistance ohmic contact may be erroneous. Control samples processed with 3409-4 indicated specific contact resistances for molybdenum on n^+InAs to be on the order of 27.3 $\Omega \cdot mm$.

4. The etching of the cap layer was an unpredictable process with respect to the etch rate. No doubt the variety of different materials in this structure contribute to this problem. Additionally, undercutting of the gate during this

self-aligned etch results in shearing at the edge of the gate contacts.

5. There may be some fundamental problems with ion implantation and high temperature annealing in a pseudomorphic heterostructure. Low energy and high dose implants have been associated with an ion beam defocusing problem, which can result in ion channeling regardless of the misorientation of the sample. Also, the possibility of dislocation induced diffusion during rapid annealing exists.

6. Some amount of inconsistent alloying of the source and drain contacts was observed. This is attributed to the inability of the germanium eutectic to diffuse because of the amorphous nature of the underlying implanted regions.

Recommendations

1. The first recommendation deals with the primary problem. More consideration needs to be given to the MBE growth process and insuring that the materials meet the specifications of the design. Given the results from this effort, this should be done before attempting to fabricate any more devices. Data from SIMS, TEM, Auger, or photoluminescense would prove useful here.

2. Since the contact resistance of molybdenum on n^+ InAs is questionable, a heavily doped GaAs cap layer could be employed. The IBM team demonstrated that this works with a molybdenum gate contact. This would lower the threshold voltage considerably. However it would also allow the pursuit

of Reactive Ion Etching (RIE) of the cap layer. This would provide better controllability of the cap etch as well, and potentially the ability to control the gate undercutting.

3. The use of a 40% AlAs mole fraction could be considered for the barrier layer even though this reduces the barrier to gate leakage and changes the threshold voltage. The reason for this is that a good quality 40% AlGaAs alloy is easier to produce than a 50% alloy.

4. Pseudomorphic structures are necessarily thin layers because of the critical thicknesses involved. Since the low energy implants may still channel (beam defocusing), the idea of a SiN implant mask over the whole structure is worth considering. This would aid in achieving a range near the channel layer and perhaps reduce damage to the implanted regions.

5. Because of the fundamental (stability) problem that may exist with the implantation and annealing of a pseudomorphic heterostructure, the possibility of a MBE re-growth technique should be investigated. MBE re-growth has been successfully demonstrated on Heterojunction Bipolar Transistors (HBTs) at the University of Illinois. The idea would be to etch the structure, after gate deposition, down past the channel layer. The doped source and drain regions would then be regrown on top of the structure.

5. Given sufficient material, control samples could be used judiciously. Specifically, a control sample would not

undergo gate metal evaporation, but undergo the cap etch, implantation, and annealing. SIMS, C-V, and four-point probe measurements would then provide a check on the implantation and annealing conditions.

6. Finally, the use of a mask set more conducive to SISFET fabrication should be considered. The mesa isolation pattern used here only protected the active area. Thus the gate pads are seriously attacked during a mesa etch.

Appendix A

First Order Charge Control Model for a self-aligned, strained-channel, n^+-InAs/Undoped $Al_{0.5}Ga_{0.5}As$/Undoped $In_{0.15}Ga_{0.85}As$ Semiconductor Insulator Semiconductor FET (SISFET)

Introduction

The simplest way to begin modelling the behavior of a SISFET is to obtain the one dimensional solution to the sheet density of electrons in the quantum well channel as a function of the applied gate voltage. The structure analyzed in this appendix is shown in Figure 42. It consists of a molybdenum gate placed on a degeneratively doped n^+-InAs cap layer. Below this layer is an undoped $Al_{0.5}Ga_{0.5}As$ barrier layer and then an undoped $In_{0.15}Ga_{0.85}As$ channel layer. The channel is grown on a 1 μm GaAs buffer layer and a semi-insulating GaAs substrate. The information here is theoretical. It is presented as an appendix because the SISFETs fabricated in this study did not work as expected. Thus, this effort does not experimentally verify the predictions from this model.

Assumptions

The following analysis is based on certain assumptions. These are listed explicitly below:

1) All available donors and acceptors are ionized in the AlGaAs under the gate, and therefore the mobile carrier densities are negligible in this region.

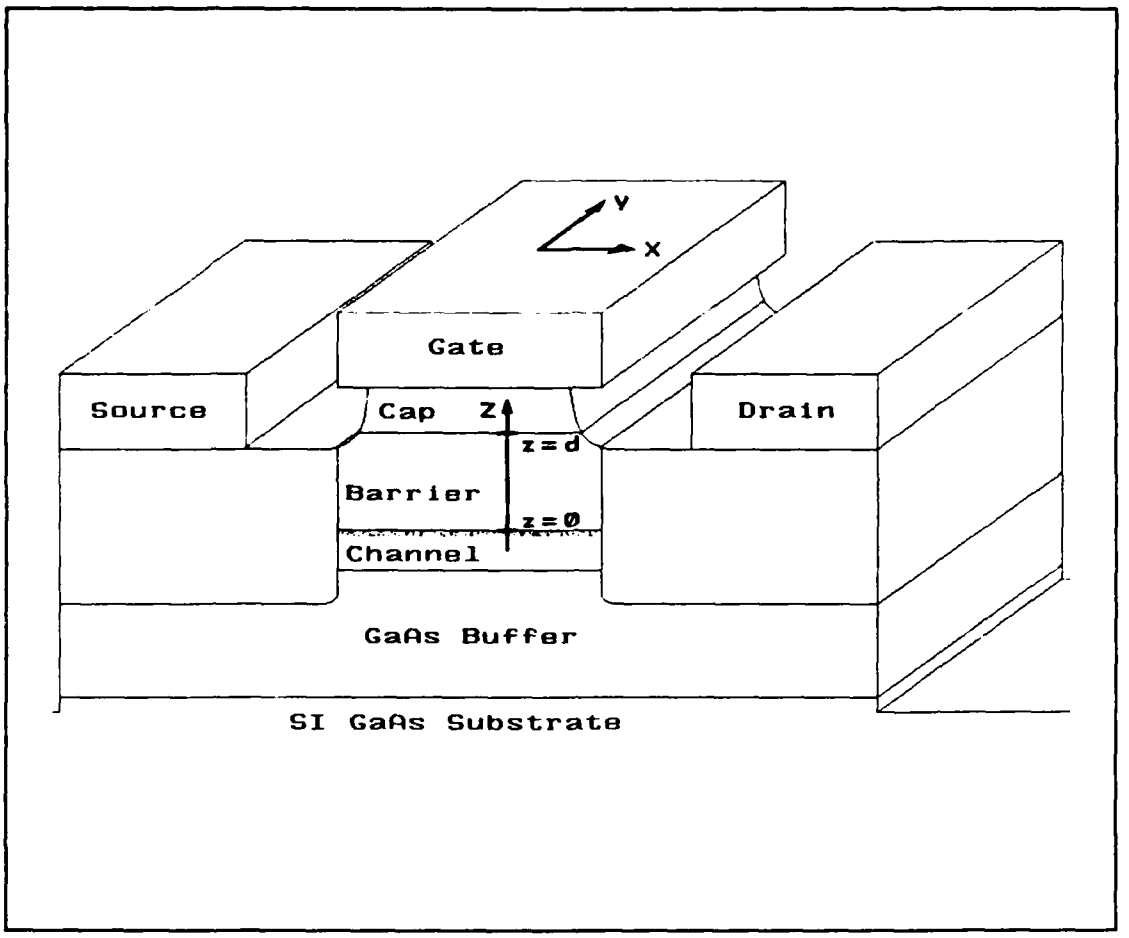


Figure 42. Coordinate System Definition for Charge Control Derivation in the SISFET Structure

2) The AlGaAs is slightly n type so that the charge in this region is ionized donors only.

3) The electric field under the gate is quasi-constant with respect to the x and y directions.

4) The potential barrier ϕ_B at the AlGaAs/InGaAs heterojunction is equal to $\phi_2 - E_{fi}$, where ϕ_2 is the AlGaAs/InGaAs conduction band discontinuity and E_{fi} is the

energy difference (volts) between the Fermi energy level and the bottom of the quantum potential well at the heterointerface.

5) The Fermi energy level in the n^+-InAs is at the conduction band (an ohmic gate contact) so that any applied gate voltage is applied directly to the InAs.

6) The pseudomorphic approximation is valid, and that each region contains a uniform crystalline structure.

7) The potential energy function of an electron just into the InGaAs channel region is approximately linear. In other words, the electric field with respect to z, where z is just less than zero, is quasi-constant and equal to E_z at the InGaAs side of the heterointerface ($z=0^-$).

In the SISFET, ideally all current is carried by the 2DEG. The following analysis ignores the possibility of parasitic conduction either in the undoped AlGaAs barrier layer or in the undoped GaAs buffer layer.

Charge Control Derivation

The equations proceed as follows. The electric field (through the surface area under the gate) in the AlGaAs as a function of z is found from Gauss' Law. Secondly, the potential energy of an electron in the AlGaAs as a function of z is found from the definition of the potential difference.

Electric Field. The electric field in the SISFET results from the spatial separation of ionized donors either in the

AlGaAs or in the implanted source and drain regions from the electrons trapped in the quantum well [29]. In general, this can be written as:

$$\mathbf{E} = E_x \cdot \mathbf{x} + E_y \cdot \mathbf{y} + E_z \cdot \mathbf{z} \qquad \text{(V/cm)}$$

From Gauss' Law: $\oint_s \mathbf{D} \cdot d\mathbf{s} = Q$

where: $\mathbf{D} = \epsilon \mathbf{E}$ (Coul/cm^2)

Q = charge enclosed (Coul)

The first step is to find the electric field perpendicular to the AlGaAs/InGaAs heterointerface as a function of the sheet carrier density n_s. This is the case because the eventual goal is to find how an applied (perpendicular) field affects the sheet carrier density. Therefore:

$$d\mathbf{s} = \mathbf{z} \cdot ds$$

Furthermore, the charge enclosed by the area (A) under the gate, in the InGaAs channel just below the heterojunction at the position $z=0^-$ is:

$$Q = -q \cdot n_s \cdot A$$

After substituting for $\mathbf{D}$, $d\mathbf{s}$, and Q, the equation for Gauss' Law becomes:

$$\oint_s \epsilon_{In} \cdot (E_x \cdot \mathbf{x} + E_y \cdot \mathbf{y} + E_z \cdot \mathbf{z}) \cdot \mathbf{z} \, ds = -q \cdot n_s \cdot A$$

where ϵ_{In} is the permittivity of y=0.15 InGaAs. After taking the dot products, and assuming E_z is constant with respect to x and y, the equation simplifies to:

$$\epsilon_{In} \cdot E_z \cdot \oint_s ds = \epsilon_{In} \cdot E_z \cdot A = -q \cdot n_s \cdot A$$

$$\epsilon_{In} \cdot E_z = -q \cdot n_s$$

Solving for E_z:

$$E_z = -q \cdot n_s / \epsilon_{In} \qquad \text{(V/cm)} \qquad \text{(for } z=0^-\text{)}$$

Applying the principle of the continuity of the tangential electric displacement vector across the heterojunction (where z=0), the electric field at $z=0^+$ (in the AlGaAs) is:

$$E_z(z=0^-) \cdot \epsilon_{In} = E_z(z=0^+) \cdot \epsilon_{Al}$$

where ϵ_{Al} is the permittivity of x=0.5 AlGaAs. After substitution and rewriting:

$$E_z = -q \cdot n_s / \epsilon_{Al} \qquad \text{(for } z=0^+\text{)}$$

This serves as the boundary condition for the next step, which is to solve for the electric field in the AlGaAs as a function of z. Again, from Gauss' Law, after substituting for D, ds, and $Q = +q \cdot N_D \cdot z \cdot A$, the equation becomes:

$$\oint_s \epsilon_{Al} \cdot (E_x \cdot \mathbf{x} + E_y \cdot \mathbf{y} + E_z \cdot \mathbf{z}) \cdot \mathbf{z} \; ds = +q \cdot N_D \cdot z \cdot A$$

Again, assuming E_z is constant with respect to x and y, the equation simplifies to:

$$\epsilon_{Al} \cdot E_z \cdot \oint_s ds = \epsilon_{Al} \cdot E_z \cdot A = +q \cdot N_D \cdot z \cdot A$$

$$\epsilon_{Al} \cdot E_z = +q \cdot N_D \cdot z$$

Solving for E_z:

$$E_z = +q \cdot N_D \cdot z / \epsilon_{Al} \qquad \text{(for } 0 \le z \le d\text{)}$$

applying the boundary condition for $E_z(z=0^+)$:

$$E_z = +q \cdot N_D \cdot z / \epsilon_{Al} - q \cdot n_s / \epsilon_{Al} \qquad \text{(for } 0 \le z \le d\text{)}$$

rewriting:

$$\mathbf{E}_z(z) = E_z \cdot \mathbf{z} = -E_z \cdot (-\mathbf{z})$$

In other words, the magnitude of the electric field in the negative z direction (-**z**) is equal to $-E_z$.

Potential. Solving for the potential energy of an electron in the AlGaAs yields the value of the conduction band energy in this region. The energy per coulomb required to move a negative charge (electron) from some initial point to a position z somewhere in the AlGaAs along a path ($\mathbf{dl} = \mathbf{z} \cdot dz$) is defined as:

$$V(z) = \int \mathbf{E} \cdot \mathbf{dl}$$

$$= \int (E_x \cdot \mathbf{x} + E_y \cdot \mathbf{y} + E_z \cdot \mathbf{z}) \cdot \mathbf{z}\, dz$$

$$V(z) = \int E_z\, dz$$

This equation is an indefinite integral form, but a solution requires a definite integral as well as a consideration of the initial conditions. For the InGaAs channel region, substituting for $E_z(z=0^-)$ from the previous sub-section and integrating from -z to 0, the result is:

$$V(z) \approx - \frac{q \cdot n_s \cdot z}{\epsilon_{In}} + \text{constant} \qquad (V) \qquad (100\text{Å} \leq z \leq 0)$$

Applying the initial condition that $V(z=0^-) = -E_{fi}$, the equation becomes:

$$V(z) \approx - \frac{q \cdot n_s \cdot z}{\epsilon_{In}} - E_{fi} \qquad (V) \qquad (100\text{Å} \leq z \leq 0)$$

For the AlGaAs barrier region, substituting for $E_z(z=0^+)$ from the previous sub-section and integrating from 0 to +z, the result is:

$$V(z) = \frac{q \cdot N_D \cdot z^2}{2 \cdot \epsilon_{Al}} - \frac{q \cdot n_s \cdot z}{\epsilon_{Al}} + \text{constant} \qquad (\text{for } 0 \leq z \leq d)$$

Applying the initial condition that $V(z=0^+) = \phi_B = \phi_2 - E_{fi}$, the equation becomes:

$$V(z) = \frac{q \cdot N_D \cdot z^2}{2 \cdot \epsilon_{Al}} - \frac{q \cdot n_s \cdot z}{\epsilon_{Al}} + \phi_2 - E_{fi} \qquad (\text{for } 0 \leq z \leq d)$$

The value of V(z) increases for increasing electron energy so that this function is equal to the conduction band energy in the AlGaAs with respect to Fermi energy level. In order to equate this result to an applied gate potential, we use the value of V at the InAs gate contact. Evaluating:

$$V(z=d) = \frac{q \cdot N_D \cdot d^2}{2 \cdot \epsilon_{Al}} - \frac{q \cdot n_s \cdot d}{\epsilon_{Al}} + \phi_2 - E_{fi} \qquad (V)$$

Since in general, potential difference is defined in terms of a positive test charge, the electron potential at the gate is equal to negative of the applied gate voltage ($-V_G$). It is also necessary to account for the conduction band discontinuity (ϕ_1) at the InAs/AlGaAs heterointerface. Thus, it is known that:

$$V(z=d) = \phi_1 - V_G$$

Equating these two results yields:

$$\phi_1 - V_G = \frac{q \cdot N_D \cdot d^2}{2 \cdot \epsilon_{Al}} - \frac{q \cdot n_s \cdot d}{\epsilon_{Al}} + \phi_2 - E_{fi} \qquad (V)$$

By defining $V_T \equiv \phi_1 - \phi_2 - (q \cdot N_D \cdot d^2)/(2 \cdot \epsilon_{Al})$, this equation becomes:

$$V_T - V_G = -q \cdot n_s \cdot d/\epsilon_{Al} - E_{fi}$$

Solving for n_s:

$$q \cdot n_s \cdot d/\epsilon_{Al} = V_G - V_T - E_{fi}$$

$$n_s = \frac{\epsilon_{Al}}{q \cdot d} \cdot [V_G - V_T - E_{fi}] \qquad (cm^{-2})$$

Summary

The equation directly above is the equation for the sheet carrier density as a function of the applied gate voltage. The above expression also reveals that a slightly more accurate expression for the threshold voltage is $V_T + E_{fi}$. This is not a closed form solution for n_s because E_{fi} is not a constant with respect to n_s. The other relationship between n_s and E_{fi} was presented in Chapter II, where n_s is a function of the allowed energy levels in the quantum well as given by the Airy equation. Thus, in order to determine either n_s or E_{fi} for a given value of V_G, it is necessary to simultaneously solve both the above equation and the following equation from the Fermi-Dirac statistics as given in Chapter II.

$$n_s = \frac{D \cdot k_B \cdot T}{q} \cdot \sum_{n=0}^{n=1} \ln \left[1 + \exp\left[\frac{q \cdot (E_{fi} - E_n)}{k_B \cdot T} \right] \right] \qquad (cm^{-2})$$

This is done for different values of V_G in Appendix B.

Appendix B

Computer Calculations of Charge Control for a self-aligned, strained-channel, n^+-InAs/Undoped $Al_{0.5}Ga_{0.5}As$/Undoped $In_{0.15}Ga_{0.85}As$ Semiconductor Insulator Semiconductor FET (SISFET)

Introduction

The calculations presented here are based on the charge control derivation in Appendix A and the equation for n_s in Chapter II. The computer software used to produce these results was MathCad Version 2.0. The approach is to simplify the Airy equation by substituting $-q \cdot n_s/\epsilon_{in}$ for E_z. The Airy equation is then rewritten in the form:

$$E_n = \alpha_n \cdot (n_s)^{2/3}$$

where:

$$\alpha_n = (\hbar^2/2 \cdot m)^{1/3}[3 \cdot \pi \cdot q^2 \cdot (n + \tfrac{3}{4})/(2 \cdot \epsilon_{in})]^{2/3} \qquad (V \cdot m^{4/3})$$

The following calculations then consider that for device modelling, there are only two relevant energy levels. Thus, only n=0 and n=1 are considered.

Assumptions

The following analysis is based on certain assumptions. These are listed explicitly below:

1) The values of α_0 and α_1 can be calculated using the value of the effective mass. However the values used are those estimated for undoped GaAs from Shubnikov-de Haas

and cyclotron resonance data for a quasi-triangular potential well [53:519].

2) The value of the density of states (D) used is measured from the cyclotron effective mass in GaAs for a quasi-triangular potential well [53:520].

3) The band gap energy of InAs is 0.36 eV and of AlGaAs is 2.05 eV for x=0.5. The analysis assumes that $q \cdot \phi_1$ equals 65% of the difference or 1.10 eV [1;2].

4) The band gap energy of x=0.5 AlGaAs is 2.05 eV and of y=0.15 InGaAs is 1.19 eV. The analysis assumes that $q \cdot \phi_2$ equals 65% of the difference or 0.56 eV [1;2].

5) The relative permittivity of x=0.5 AlGaAs is 11.6 and of y=0.15 InGaAs is 13.4.

6) The background concentration of donors in the AlGaAs is N_D, and it equals 10^{15} cm^{-3}.

Calculations

The following calculations start with unit definitions. Second, using a solve block, the two equations for n_s as a function of E_{fi} are solved simultaneously. The equations are solved for 12 values of V_G ranging from 0.0 volts to 5.5 volts. The results are plots of: n_s as a function of V_G, ϕ_B as a function of V_G, and the conduction band in the AlGaAs for a forward biases, V_G, equal to 0.0, 1.0, and 2.0 volts. The next six pages are a printout of the actual MathCad document used to perform the calculations.

First, define all units and material parameters:

$cm \equiv 1L \qquad m \equiv 100\,cm \qquad K \equiv 1 \qquad coul \equiv 1Q$

$A \equiv 10^{-10}\,m \qquad gm \equiv 1M \qquad kg \equiv 1000\,gm \qquad sec \equiv 1T$

$$joule \equiv \frac{kg\,m^2}{sec^2} \qquad volt \equiv \frac{joule}{coul} \qquad farad \equiv \frac{coul}{volt}$$

$eV \equiv 1.6\,10^{-19}\,joule \qquad q := 1.6\,10^{-19}\,coul \qquad d := 500\,A$

$$\epsilon_o := 8.85\,10^{-14}\,\frac{farad}{cm} \qquad \epsilon_{Al} := 11.6\,\epsilon_o \qquad \epsilon_{In} := 13.4\,\epsilon_o$$

$\phi_1 := 1.10\,volt \qquad \phi_2 := 0.56\,volt \qquad N_D := 10^{15}\,cm^{-3}$

$D := 3.24\,10^{17}\,m^{-2}\,volt^{-1} \qquad k_B := 1.38\,10^{-23}\,\frac{joule}{K}$

$$V_T := \phi_1 - \phi_2 - \frac{q\,N_D\,d^2}{2\,\epsilon_{Al}} \qquad T := 300\,K$$

$$F := \frac{k_B\,T}{q} \qquad V_T = 0.538\,volt$$

$$\alpha_o := 2.5\,10^{-12}\,volt\,m^{\frac{4}{3}} \qquad \alpha_1 := 3.2\,10^{-12}\,volt\,m^{\frac{4}{3}}$$

Second, perform simultaneous solution of the two equations:

Initial Guess
for Solve Routine:

$$n := 5\ 10^{12}\ cm^{-2} \qquad E := -0.5\ volt$$

Given

$$n \approx D\ F\left[\ln\left[1 + \exp\left[\frac{E - \propto_o n^{\frac{2}{3}}}{F}\right]\right] + \ln\left[1 + \exp\left[\frac{E - \propto_1 n^{\frac{2}{3}}}{F}\right]\right]\right]$$

$$n \approx \frac{\epsilon_{Al}}{q\ d}\left[V - V_T - E\right]$$

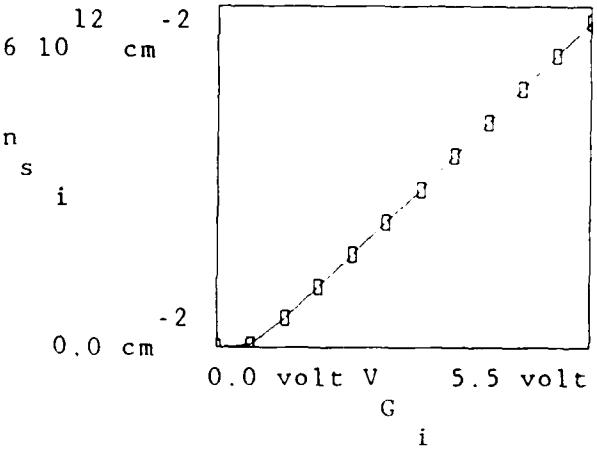
f(V) := Find(n,E)

$$V_G := \begin{bmatrix} 0.0 \\ 0.5 \\ 1.0 \\ 1.5 \\ 2.0 \\ 2.5 \\ 3.0 \\ 3.5 \\ 4.0 \\ 4.5 \\ 5.0 \\ 5.5 \end{bmatrix} volt \qquad i := 0,1\ ..11$$

$$B^{\langle i \rangle} := f\left[\begin{matrix} V_G \\ i \end{matrix}\right]$$

$$n_{s_i} := B_{0,i}\ cm^{-2}$$

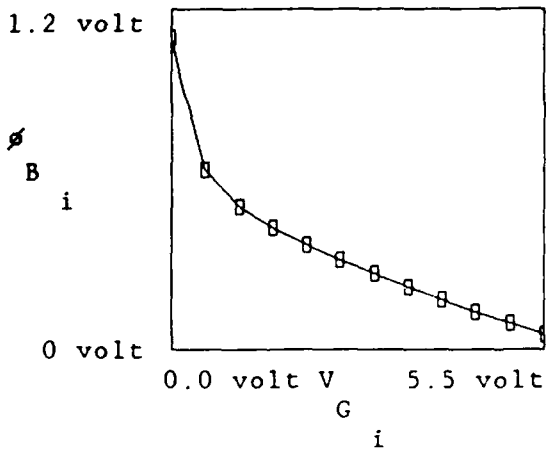
Plot carrier sheet density versus applied gate voltage.



Now, plot the barrier to gate leakage versus gate voltage:

$$E_{fi_i} := B_{1,i}\ gm\ cm^{2}\ sec^{-2}\ coul^{-1}$$

$$\phi_{B_i} := \phi_{2_i} - E_{fi_i}$$



Graph conduction band for various values of gate voltage:

$$V(z) := \frac{q\,N_D\,z^2}{2\,\epsilon_{Al}} - \frac{q\,n_s\,z}{\epsilon_{Al}} + \phi_2 - E_{fi} \qquad \text{For z from z=0 to z=d}$$

Define range from 0 to d as AlGaAs:

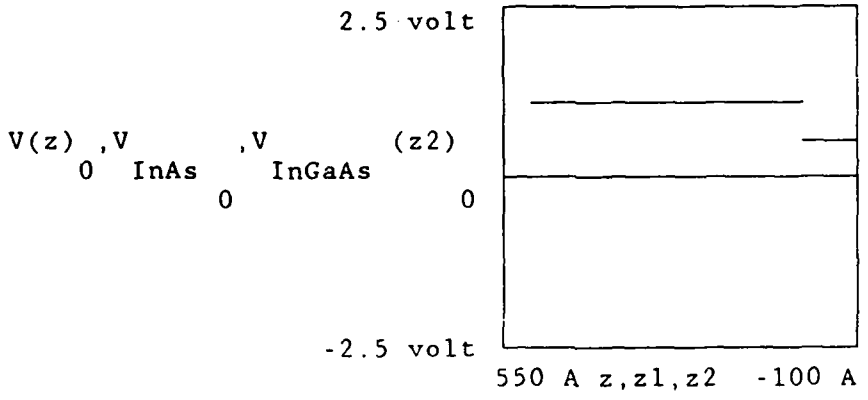
$$z := 0\,A, 20\,A\,..d$$

Define potential at ranges just into InAs and InGaAs as:

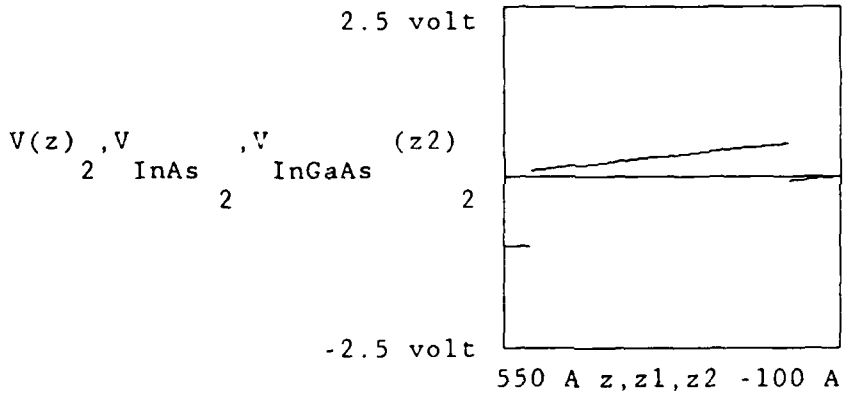
$$V_{InAs} := V(d) - \phi_1 \qquad z1 := d, d + 10\,A\,..550\,A$$

$$V_{InGaAs}(z) := -\left[\frac{q\,n_s\,z}{\epsilon_{In}}\right] - E_{fi} \qquad z2 := -100\,A, -90\,A\,..0\,A$$

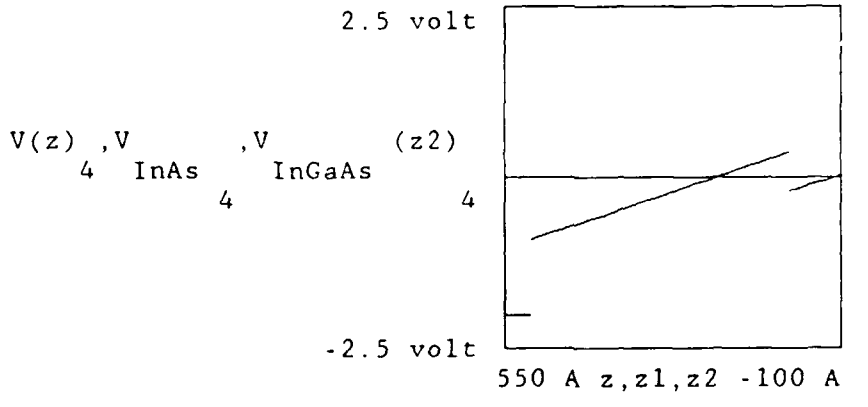
The following plots are conduction band diagrams for values of gate voltage at 0, 1, and 2 volts. All voltages are with respect to the Fermi energy level in the InGaAs channel (V=0).



Gate Voltage Equals 0.0 volts



Gate Voltage Equals +1.0 volts



Gate Voltage Equals +2.0 volts

$\mu m \equiv 10^{-6}\ m$ $\quad mA \equiv 10^{-3}\ \frac{coul}{sec}$ Define units to plot I-V curves with a 2 piece linear approximation

$L := 2\ \mu m$ $\quad W := 100\ \mu m$ Define typical transistor length and width

$\mu := 7000\ \frac{cm^2}{volt\ sec}$ $\quad v_s := 1.33\ 10^7\ \frac{cm}{sec}$ Low field mobility & saturation velocity

$E_s := \frac{v_s}{\mu}$ $\quad E_s = 1.9\ 10^3\ \frac{volt}{cm}$ Saturation field

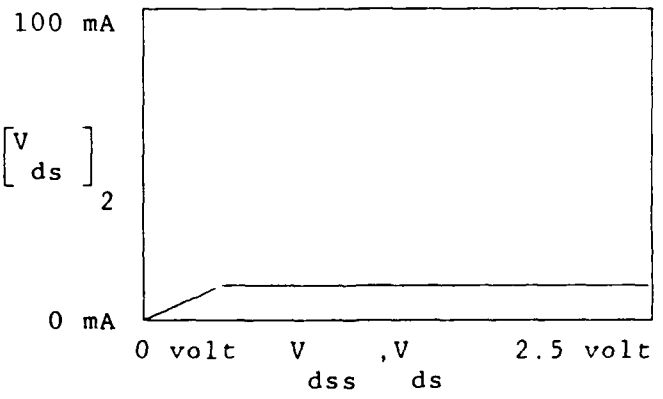
$V_o := E_s\ L$ $\quad V_o = 0.38\ volt$ Vds at saturation

$I_{dss} := q\ n_s\ v_s\ W$ Maximum saturation current assuming source resistance equals zero

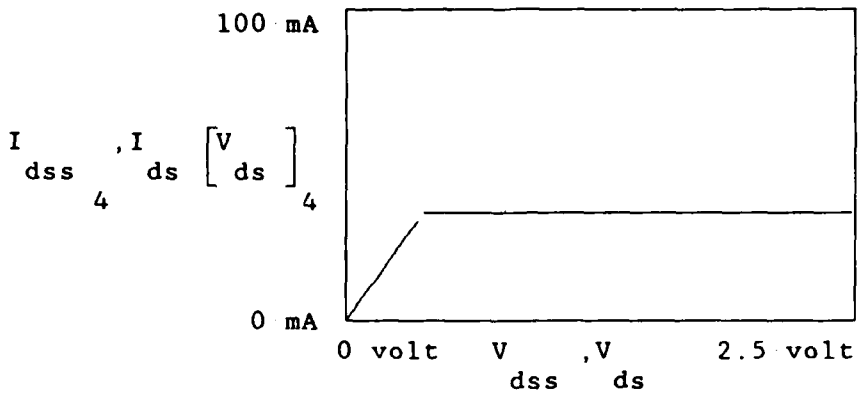
$I_{ds}(v) := q\ n_s\ \mu\ \frac{v}{L}\ W$ Ids for Vds in linear region, low field mobility is constant

$V_{ds} := 0\ volt, 0.05\ volt\ ..V_o$ Linear region

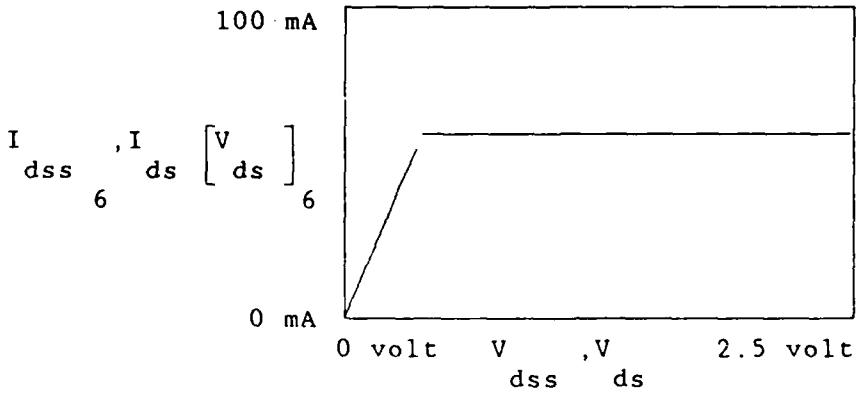
$V_{dss} := V_o, V_o + 0.05\ volt\ ..2.5\ volt$ Saturation region



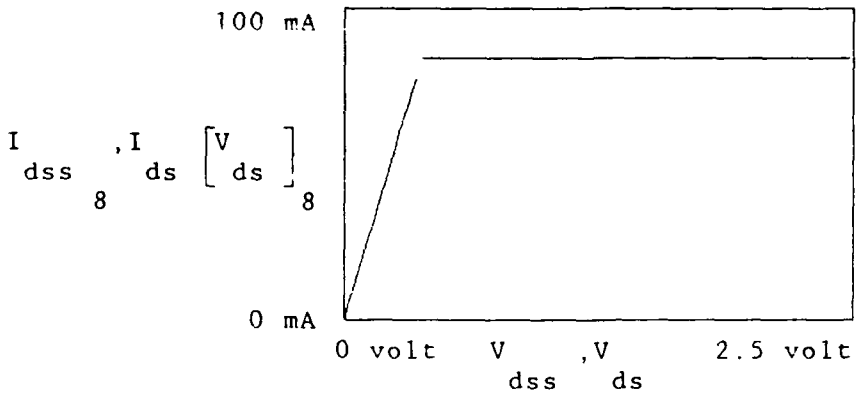
Gate voltage equals +1.0 volts



Gate voltage equals +2.0 volts



Gate voltage equals +3.0 volts



Gate voltage equals +4.0 volts

Summary

The preceding calculations support the presupposition that a pseudomorphic SISFET, with the design parameters attempted in this study, would have a positive threshold voltage. The first plot of sheet carrier density versus shows that the concentration in the channel does not, according to these calculations, reach sufficient magnitude (i.e. 5×10^{11} cm^{-2} or greater) until approximately one volt forward bias is applied to the gate. Furthermore, the barrier to gate leakage, ϕ_B, would be much improved over the standard SISFET. The second plot of barrier versus gate voltage predicts that even at three volts forward gate bias, ϕ_B should be approximately 0.3 volts. By comparison, the calculations reveal a barrier of approximately 0.6 volts at threshold whereas the barrier in a standard SISFET at threshold is slightly less than 0.3 volts. The conduction band diagrams indicate how the barrier becomes more trapezoidal in nature as greater forward bias is applied. And finally, the simple two piece linear approximation provides maximum estimates for the I-V characteristics of the pseudomorphic SISFET under forward bias.

Bibliography

1. Adachi, S. "GaAs, AlAs, and $Al_xGa_{1-x}As$: Material Parameters for Use in Research and Device Applications," Journal of Applied Physics, 58: R1-R29 (August 1985).

2. Adachi, S. "Material Parameters of $In_{1-x}Ga_xAs_yP_{1-y}$ and Related Binaries," Journal of Applied Physics, 53: 8775-8792 (December 1982).

3. Arnold, D. J., R. Fischer, W. F. Kopp, T. S. Henderson, and H. Morkoç. "Microwave Characterization of (AlGa)As/GaAs Modulation Doped FETs: Bias Dependence on Small Signal Parameters," IEEE Transactions on Electron Devices, 31: 1399-1402 (October 1984).

4. Chen, J., PhD Candidate in Electrical Engineering, University of Illinois at Urbana-Champagne. Personal Interview. University of Illinois, Coordinated Sciences Laboratory, 28 June 1988.

5. Cirillo, N. C., J. K. Abrokwah, and M. S. Shur. "Self-Aligned Modulation-Doped AlGaAs/GaAs Field-Effect Transistors," IEEE Electron Device Letters, 5: 129-131 (April 1984).

6. Cirillo, N. C., M. S. Shur, P. J. Vold, J. K. Abrokwah, and O. N. Tufle. "Realization of n-Channel and p-Channel High Mobility AlGaAs/GaAs Heterostructure Insulating Gate FET's on a Planar Wafer Surface," IEEE Electron Device Letters, 6: 645-647 (December 1985).

7. Crist, J., Lead Engineer for Implantation and Annealing, Air Force Wright Aeronautical Laboratories. Personal Interviews. Wright-Patterson AFB Ohio, February through November 1988.

8. Cullity, B. D. Elements of X-Ray Diffraction. Reading, Massachusetts: Addison-Wesley, 1967.

9. Davenport, Wilbur B. Probability and Random Processes: An Introduction for Applied Scientists and Engineers. New York: McGraw-Hill, 1970.

10. Delagebeaueuf, D. and N. T. Linh. "Charge Control of the Heterojunction Two-Dimensional Electron Gas for MESFET Application," IEEE Transactions on Electron Devices, 28: 790-795 (July 1981).

11. Drummond, T. J., H. Morkoç, K. Lee, and M. S. Shur. "Model for Modulation Doped Field Effect Transistor," IEEE Electron Device Letters, 3: 338-341 (November 1982).

12. Drummond, T. J., W. T. Masselink, and H. MorkoÇ. "Modulation Doped GaAs/AlGaAs Heterojunction Field Effect Transistors: MODFETS," Proceedings of the IEEE, 74: 773-822 (June 1986).

13. Edington, J. W. Practical Electron Microscopy in Materials Science. New York: Van Nostrand Reinhold Company, 1976.

14. Feuer, M.D., T. Y. Chang, and S. C. Shunk. "InGaAs/InAlAs Heterostructure Diodes for Application to High-Speed Semiconductor Gated FET's," IEEE Transactions on Electron Devices, 33: 1640-1643 (November 1986).

15. Feuer, M. D., T. Y. Chang, S. C. Shunk, and B. Tell. "Semiconductor-Gated InGaAs/InAlAs Heterostructure Transistors (SISFETs)," IEEE Electron Device Letters, 8: 33-35 (January 1987).

16. Feuer, M. D., J. M. Kuo, S. C. Shunk, R. E. Behringer, and Tao-Yuan Chang. "Microwave Performance of InGaAs/InAlAs/InP SISFETs," IEEE Electron Device Letters, 9: 162-164 (April 1988).

17. Fischer, R., T. J. Drummond, J. Klem, W. Kopp, T. S. Henderson, D. Perrachione, and H. MorkoÇ. "On the Collapse of Drain I-V Characteristics in Modulation-Doped FET's at Cryogenic Temperatures," IEEE Transactions on Electron Devices, 31: 1028-1032 (August 1984).

18. Gabriel, B. L. SEM: A USer's Manual for Materials Science. Metals Park, Ohio: American Society for Metals, 1985.

19. Gibbons, James F. "Ion Implantation in Semiconductors - Part I: Range Distribution Theory and Experiments," Proceedings of the IEEE, 56: 295-320 (March 1968).

20. Gibbons, James F. "Ion Implantation in Semiconductors - Part II: Damage Production and Annealing," Proceedings of the IEEE, 60: 1062-1097 (September 1972).

21. Goldstein, J. I., and H. Yakowitz. Practical Scanning Electron Microscopy. New York: Plenum Press, 1976.

22. Hodul, David and Mahta Sandeep. "Measurement of Dynamic Temperature Uniformity in Rapid Thermal Processing," Solid State Technology, 209-211 (May 1988).

23. Heiblum, M. et al. "Characteristics of AuGeNi Ohmic Contacts to GaAs," Solid State Electronics, 25: 185-195 (March 1982).

24. Henderson, T. S., W. T. Masselink, W. Kopp, and H. Morkoç. "Determination of Carrier Saturation Velocity in High-Performance $In_yGa_{1-y}As/Al_xGa_{1-x}As$ Modulation Doped Field Effect Transistors ($0 \leq y \leq 0.2$)," IEEE Electron Device Letters, 7: 288-290 (May 1986).

25. Ishikawa, T., S. Hiyamiza, T. Mimura, J. Saito, H. Haoshimoto. "The Effect of Annealing on the Electrical Properties of Selectively Doped GaAs/n-AlGaAs Heterojunction Structures grown by MBE," Japanese Journal of Applied Physics, 20: L814-L816 (1981).

26. Katayama, Y., M. Morioka, Y. Sawada, K. Ueyanagi, T. Mishima, Y. Ono, T. Usagawa, Y. Shiraki. "A New Two-Dimensional Electron Gas Field-Effect Transistor Fabricated on Undoped AlGaAs/GaAs Heterostructure," Japanese Journal of Applied Physics, 23: L150-L152 (March 1984).

27. Kelly, M. J. and C. Weisbuch. The Physics and Fabrication of Microstructures and Microdevices, Section 3, 370-393, Berlin: Springer-Verlag, 1986.

28. Kittel, C. Introduction to Solid State Physics. New York: John Wiley and Sons, 1986.

29. Kraus, J. D. Electromagnetics. New York: McGraw-Hill, 1984.

30. Lee, H. et al. "High Temperature Annealing of Modulation-Doped AlGaAs/GaAs Heterostructures for FET Applications," Proceedings of the IEEE/Cornell Conf. on High-Speed Semiconductor Devices and Circuits, 204-208 (August 1984).

31. Lee, Kwyro, M. S. Shur, T. J. Drummond, and H. Morkoç. "Parasitic MESFET in (Al,Ga)As/GaAs Modulation Doped FET's and MODFET Characterization," IEEE Transactions on Electron Devices, 31: 29-35 (January 1984).

32. Lee, Kwyro, M. S. Shur, T. J. Drummond, and H. Morkoç. "Current-Voltage and Capacitance-Voltage Characteristics of Modulation-Doped Field Effect Transistors," IEEE Transactions on Electron Devices, 30: 207-216 (March 1983).

33. Linder, Capt Scott L. The Characterization of Whiskers Produced by Electromigration on Suspended Aluminum Linestripes. MS Thesis, AFIT/GE/ENG/86D-35. School of Engineering, Air Force Institute of Technology (AU), Wright-Patterson AFB OH, December 1986.

34. Litton, C. W., Senior Scientist, Air Force Wright Aeronautical Laboratories. Personal Interviews. Wright-Patterson AFB Ohio, February through November 1988.

35. Lott, Capt James A. Characterization of Enhanced Schottky Barrier InGaAs/AlGaAs Strained-Channel MODFETs. MS Thesis, AFIT/GE/ENG/87D-38. School of Engineering, Air Force Institute of Technology (AU), Wright-Patterson AFB OH, December 1987.

36. Lott, Capt James A. Lead Engineer, Sandia National Laboratories. Telephone Interviews. Wright-Patterson AFB Ohio, 14 May 1988.

37. Luscher, P. "Crystal Growth by Molecular Beam Epitaxy," Solid State Technology, 20: 43-52 (December 1977).

38. Masselink, William T. et al. "The Dependence of 77 °K Electron Velocity-Field Characteristics on Low-Field Mobility in AlGaAs/GaAs Modulation Doped Structures," IEEE Transactions on Electron Devices, 33: 639-645 (May 1986).

39. Matthews, J. W., and A. E. Blakeslee. "Defects in Epitaxial Multilayers," Journal of Crystal Growth, 27: 118-125 (July 1974).

40. McKelvey, John P. Solid State and Semiconductor Physics. New York: Harper and Row, 1966.

41. McLaughlin, 1Lt Thomas E. Fabrication of AlGaAs/InGaAs Pseudomorphic Modulation Doped Field Effect Transistors. MS Thesis, AFIT/GE/ENG/86D-11. School of Engineering, Air Force Institute of Technology (AU), Wright-Patterson AFB OH, December 1986.

42. Matsumoto, K., M. Ogura, T. Wada, N. Hashizume, T. Yao, Y. Hayashi. "n^+-GaAs/Undoped-GaAlAs/Undoped-GaAs Field Effect Transistor," Electronics Letters, 20: 462-463 (May 1984).

43. Mishra, U. K., S. C. Palmateer, P. C. Chao, P. M. Smith, and J. C. M. Hwang. "Microwave Performance of 0.25 micro-meter Gate Length High Electron Mobility Transistors," IEEE Electron Device Letters, 6: 142-145 (March 1985).

44. Morkoç, Hadis and Paul M. Solomon. "The HEMT: A Superfast Transistor," IEEE Spectrum, 21: 28-35 (February 1984).

45. Morkoç, Hadis in E. H. C. Parker Ed. The Technology and Physics of Molecular Beam Epitaxy, Chapter 7. New York: Plenum Press, 1985.

46. Morkoç, Hadis., Professor of Electrical Engineering, University of Illinois at Urbana-Champagne. Personal Interview. University of Illinois, Coordinated Sciences Laboratory, 28 June 1988.

47. Peng, C. K., J. Chen, J. Chyi, and H. Morkoç. "Extremely Low Non-Alloyed and Alloyed Contact Resistance Using an InAs Cap Layer on InGaAs by Molecular Beam Epitaxy," Report to CSL Personnel, University of Illinois, Urbana, Illinois, July 1988.

48. Ponse, F., W. T. Masselink, and H. Morkoç. "Quasi-Fermi Level Bending in MODFETs and Its Effect on FET Transfer Characteristics," IEEE Transactions on Electron Devices, 32: 1017-1023 (June 1985).

49. Priddy, K. L., D. R. Kitchen, J. A. Grzyb, C. W. Litton, T. S. Henderson, C. K. Peng, W. F. Kopp, and H. Morkoç. "Design of Enhanced Schottky-barrier AlGaAs/GaAs MODFET's Using Highly Doped p^+ Surface Layers," IEEE Transactions on Electron Devices, 34: 175-180 (February 1987).

50. Priddy, 1Lt Kevin L. Study and Analysis of AlGaAs/GaAs Modulation Doped Field Effect Transistors Incorporating P-Type Schottky Gate Barriers. MS Thesis, AFIT/GE/ENG/85D-1. School of Engineering, Air Force Institute of Technology (AU), Wright-Patterson AFB OH, December 1985.

51. Sandia National Laboratories, Division 1141. Memorandum on Various Etchants and Etch Rates, Kirtland AFB New Mexico, (8 June 1988).

52. Shannon, J. "Control of Schottky Barrier Height Using Highly Doped Surface Layers," Solid State Electronics, 19: 537-543 (June 1976).

53. Shur, Michael. GaAs Devices and Circuits, Chapter 10. New York: Plenum Press, 1986.

54. Solomon, P. M., C. M. Knoedler, and S. L. Wright. "A GaAs Gate Heterojunction FET," IEEE Electron Device Letters, 5: 379-381 (September 1984).

55. Solomon, P. M. and Morkoç, Hadis. "Modulation Doped GaAs/AlGaAs Heterojunction Field Effect Transistors (MODFETS), Ultra High Speed Device for Super Computers," IEEE Transactions on Electron Devices, 31: 1015-1027 (August 1984).

56. Solomon, P. M., T. W. Hickmott, H. Morkoç, and R. Fischer. "Electrical Measurements on n^+-GaAs/undoped $Al_{0.4}Ga_{0.6}As$/n-GaAs Capacitors," Applied Physics Letters, 42: 821-823 (May 1983).

57. Stern, F. and S. D. Sarma. "Electron Energy levels in GaAs-AlGaAs Heterojunctions," Physics Review, B30: 840-848 (1984).

58. Swanson, A. W. "The Pseudomorphic HEMT," Microwaves & RF, 26: 139-150 (March 1987).

59. Sze, S. M. Semiconductor Devices, Physics and Technology. New York: John Wiley and Sons, 1985.

60. Sze, S. M. Physics of Semiconductor Devices. New York: John Wiley and Sons, 1981.

61. Thomas, G. Transmission Electron Microscopy of Metals. New York: John Wiley and Sons, 1962.

62. Thomas, G. and Goringe, M. Transmission Electron Microscopy of Materials. New York: John Wiley and Sons, 1979.

63. Unlu, H. and H. Morkoç. "Strained Layer InGaAs/AlGaAs Quantum Wells for Ultrahigh Frequency MODFETs," Solid State Technology, 31: 83-87 (March 1988).

64. Vinter, B. "Subbands and Charge Control in a Two-Dimensional Electron Gas Field Effect Transistor," Applied Physics Letter, 44: 307-309 (February 1984).

VITA

Captain David W. Rapp [redacted] of American parents. He graduated from Conestoga Valley High School, Lancaster, Pennsylvania in 1980 and from Lehigh University, Bethlehem, Pennsylvania in 1984 with a Bachelor of Science in Electrical Engineering. He was a distinguished graduate of the Reserve Officers Training Corps (ROTC) and on 2 June 1984 was commissioned a Second Lieutenant in the United States Air Force. Captain Rapp was assigned to the World Wide Military Command and Control Information System (WIS) Program Office, Strategic Systems Directorate, Electronic Systems Division, Hanscom Air Force Base, Massachusetts where he served as lead engineer for the development of the backbone Local Area Network system. On 8 June 1987, he then entered the School of Engineering, Air Force Institute of Technology, Wright-Patterson Air Force Base, Ohio. He is married and has two children. Captain Rapp is a member of Tau Beta Pi and Eta Kappa Nu.

[redacted]

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1a. REPORT SECURITY CLASSIFICATION: UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release; distribution unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S): AFIT/GE/ENG/88D-40	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION: School of Engineering; 6b. OFFICE SYMBOL (If applicable): AFIT/ENG	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State, and ZIP Code): Air Force Institute of Technology, Wright-Patterson AFB OH 45433-6583	7b. ADDRESS (City, State, and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION: Electronics Research Br.; 8b. OFFICE SYMBOL (If applicable): AFWAL/AADR	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State, and ZIP Code): Air Force Wright Aeronautical Laboratories, Wright-Patterson AFB OH 45433-6583	10. SOURCE OF FUNDING NUMBERS: PROGRAM ELEMENT NO.; PROJECT NO.; TASK NO.; WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification): See Box 19

12. PERSONAL AUTHOR(S): David W. Rapp, B.S.E.E., Captain, USAF

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
MS Thesis	FROM _____ TO _____	1988 December	167

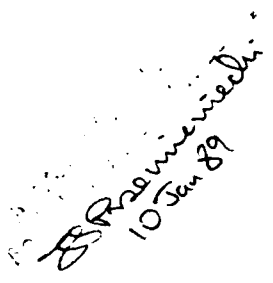
16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Heterojunction Transistors, Field Effect Transistors (FETs), Semiconductor Insulator Semiconductor FETs (SISFETs), Pseudomorphic Device Heterostructures
09	01		
20	12		

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Title: INVESTIGATION OF A SELF-ALIGNED, STRAINED-CHANNEL, n^+-InAs/$Al_{0.5}Ga_{0.5}As$/$In_{0.15}Ga_{0.85}As$ SEMICONDUCTOR INSULATOR SEMICONDUCTOR FET (SISFET)

Thesis Chairman: Donald R. Kitchen, Major, USAF
Instructor of Electrical Engineering



20. DISTRIBUTION/AVAILABILITY OF ABSTRACT: ☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION: UNCLASSIFIED
22a. NAME OF RESPONSIBLE INDIVIDUAL: Donald R. Kitchen, Major, USAF	22b. TELEPHONE (Include Area Code): (513) 255-4960; 22c. OFFICE SYMBOL: AFIT/ENG

DD Form 1473, JUN 86 — Previous editions are obsolete. — SECURITY CLASSIFICATION OF THIS PAGE

The idea of a new type of Semiconductor Insulator Semiconductor Field Effect Transistor (SISFET) device has been investigated. The attempted design consists of a heavily doped n-type InAs gate with undoped $Al_{0.5}Ga_{0.5}As$ as the gate insulator and with undoped $In_{0.15}Ga_{0.85}As$ as a strained-channel on an undoped GaAs buffer layer. SISFETs provide freedom from the Donor compleX (DX) center and have threshold voltages which are independent of the AlGaAs doping and thickness. Calculations predict that the proposed pseudomorphic structure would produce a device with a natural threshold voltage of approximately 0.6 volts. This would be well suited to digital logic applications. Calculations also predict that this new material structure would provide a barrier to gate leakage of greater than 0.3 volts up to 2.5 volts of positive gate bias. The layers were grown by MBE, and "devices" were fabricated using a self-aligned process which involved ion implantation and rapid thermal annealing. Some finished samples exhibited transistor action, but problems included inordinately high gate leakage and non-ohmic source and drain contacts. Specific contact resistance of 0.65 $\Omega \cdot mm$ was achieved, but the pseudomorphic SISFET was not successfully fabricated as expected. A TEM analysis, along with other electrical and qualitative analyses, support the conclusion that at least one of the problems was the MBE growth.